LCFC Confidential

SKYWALKER NM-A831 Rev2.0 Schematic

Intel KabyLake Processor with DDR4 + PCH-LP

NVIDIA N16S-GTR GDDR5 2GB
NVIDIA N16P-GT GDDR5 2GB

2016-08-24 Rev2.0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: COVER PAGE		
Size: Custom	Document Number: SKYWALKER	Rev: 2.0
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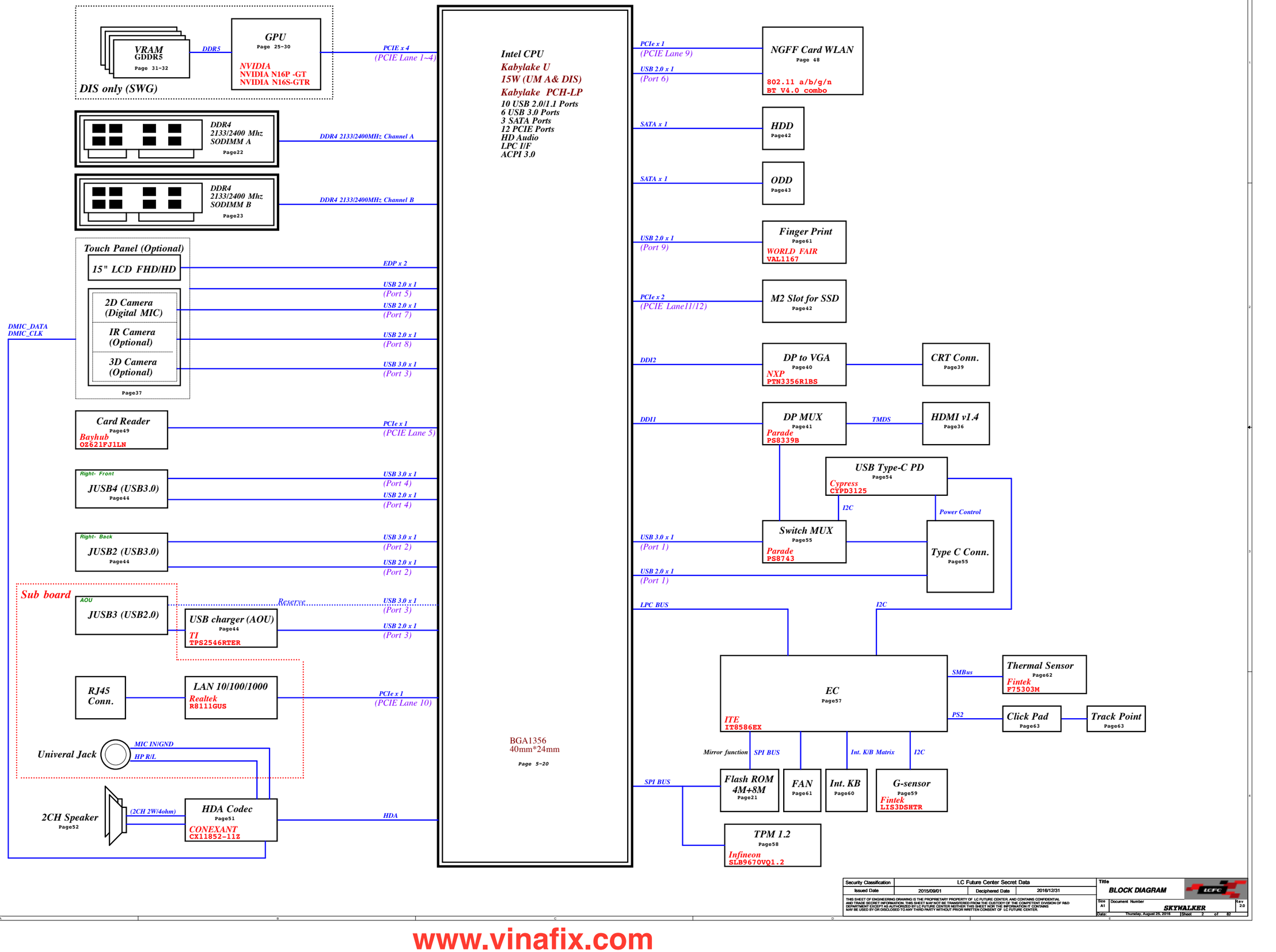
Skywalker KBL U Block Diagram



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Issued Date	2015/09/01	Deciphered Date	2016/12/31

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Title	BLOCK DIAGRAM	
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+ +3VL	+3VALW +5VALW +1VALW +1.8VALW	+2.5V +1.2V +VCC_STG	+5VS +3VS +VCC_CORE +VCC_IO +VCC_SA +VCC_ST +VGA_CORE +3VS_VGA +1.35VS_VGA +3VS_AON +1VS_VGA +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SIGNAL / STATE	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON2	EC_ON	SUSP#	SYSON
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	HIGH
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	HIGH
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF	LOW
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF	LOW

SMBUS Control Table

	SOURCE	Main VGA	BATT (Charger)	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	LAN PHY	G sensor	USB Type-C
EC_SMB_CK1 EC_SMB_DA1	IT8580F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580F +3VL	X	X	X	X	X	X	X	X	X	V +3VPD_VDD
EC_SMB_CK3 EC_SMB_DA3	IT8580F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	V +3VS_GS	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	X	X	X	X	V +5VS	X	X	X
PCH_SML1CLK PCH_SML1DAT	PCH +3V_PCH	X	X	X	X	X	X	X	X	X	X

BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
XDP@	Debug port
UMA@	UMA SKU ID
DIS@	Optimus SKU ID
DIMM2@	For DIMM2 function
DIMM1@	For DIMM1 function
TYPEC@	For USB Type-C function
ME@	ME Connector
EMC@	For EMC function
EMC_2D@	For EMC function
EMC_NS@	For EMC function
RF_NS@	For RF function
S2G@	For VRAM Strap
CHA@	For VRAMA function
CHB@	For VRAMB function
RANKA@	GPU DDR5 Setting
X76@	GPU VRAM Setting
3DCCD@	3D Camera Setting
VGA@	VGA Setting
MUX@	MUX Setting
ODD@	ODD Setting
TPM@	Trusted Platform Module (TPM)
MIRROR@	For mirror function
NGC6@	For VGA Non GC6 function
GC6@	For VGA GC6 function

USB2 Port

Port	Device
1	JUSB1 TYPE-C
2	JUSB2
3	JUSB3 Sub board
4	JUSB4
5	Touch Panel
6	BT
7	CMOS
8	IR CAMERA
9	FP/Smart

USB3 Port

Port	Device
1	JUSB1 TYPE-C
2	JUSB2
3	3D CCD
4	JUSB4

PCIE Port

Port	Device
1	GPU
2	GPU
3	GPU
4	GPU
5	CardReader
6	X
7	X
8	X
9	WLAN
10	LAN
11	M.2 SSD
12	M.2 SSD

SATA Port

Port	Device
1	HDD
2	ODD
3	X
4	X

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Title: NOTE LIST

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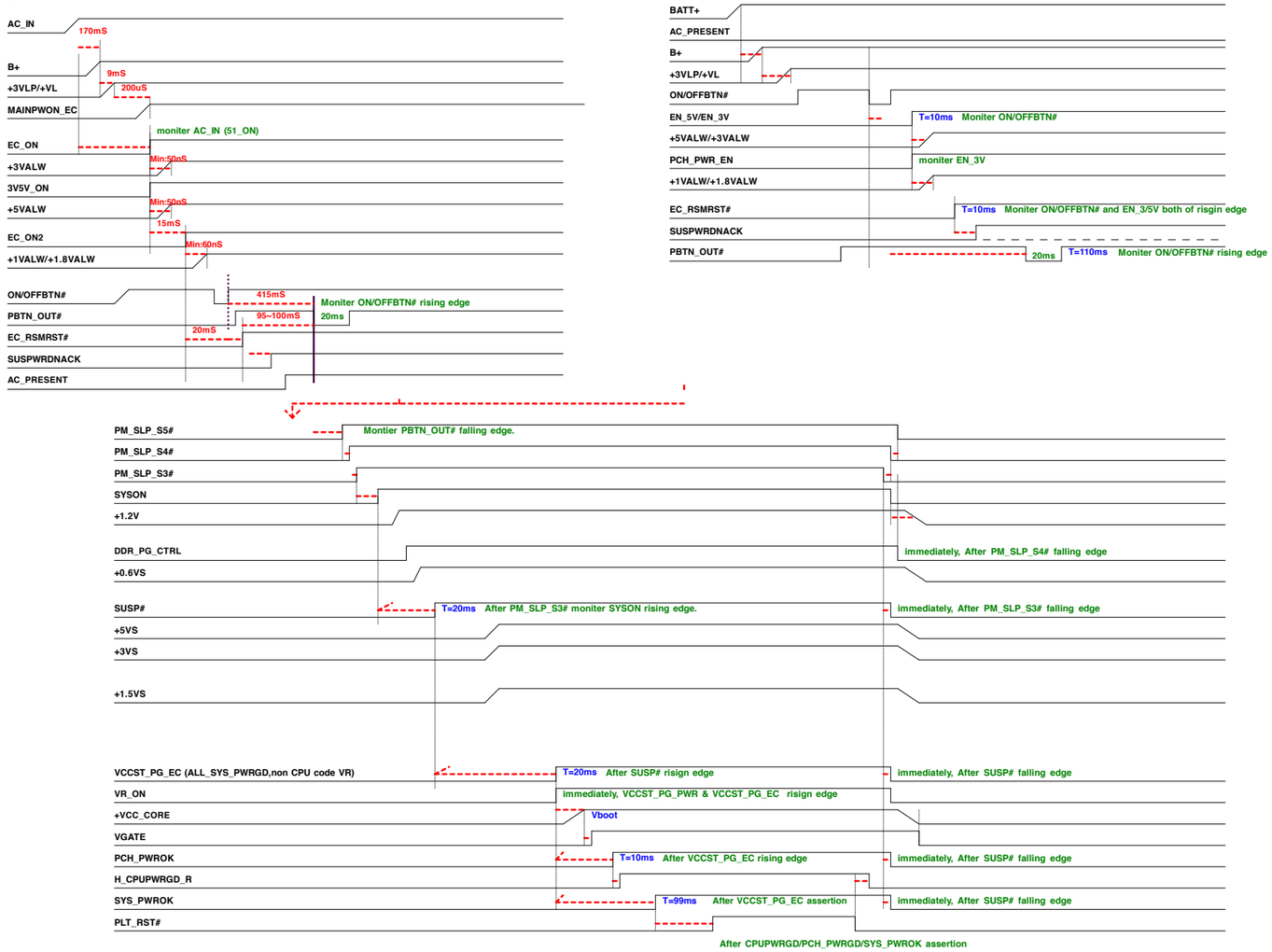
Skywalker PWR Sequence_SKL-U_DDR4_Non-Deep Sx]

[AC Mode]



[DC Mode]

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Title: Power Sequence

Size	Document Number	Rev
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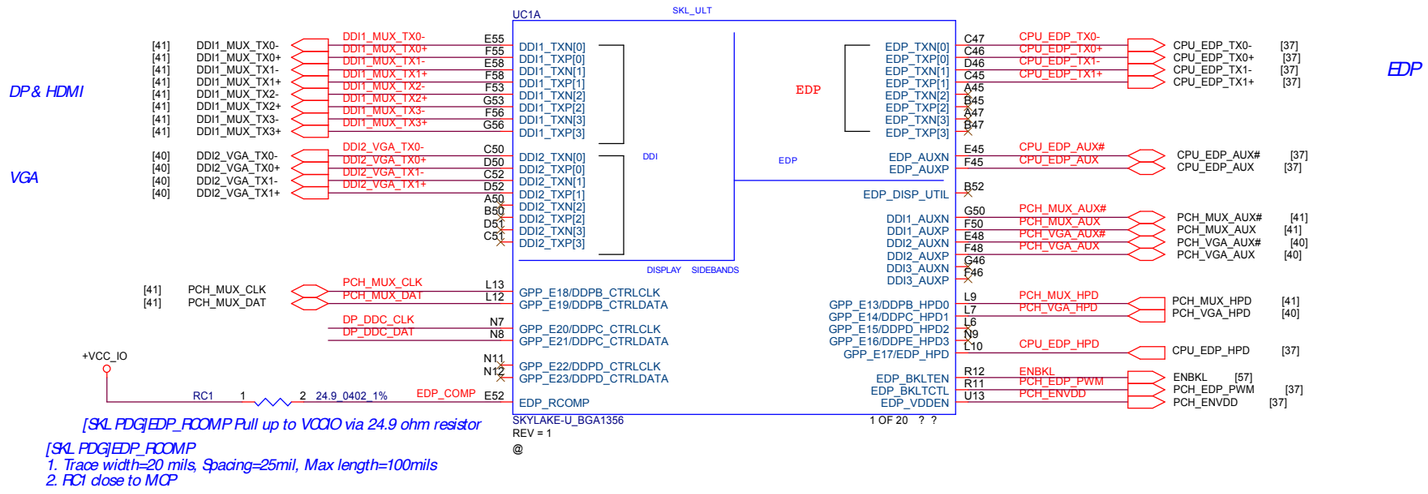
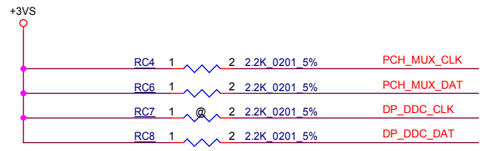


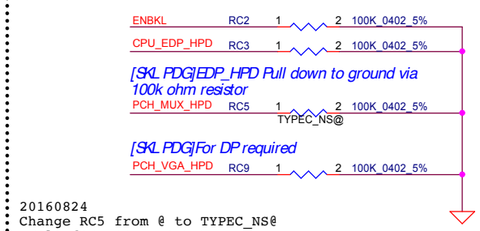
[SKL PDG]EDP_RCOMP Pull up to VCCIO via 24.9 ohm resistor

[SKL PDG]EDP_RCOMP
1. Trace width=20 mils, Spacing=25mil, Max length=100mils
2. RC1 close to MCP

DDPB_CTRLDATA, DDPC_CTRLDATA Internal PD 20K



20160202
Install RC4,RC6 to fix dual display issue



20160824
Change RC5 from @ to TYPEC_NS@
(Only for Non Type-C SKU)

DDPB_CTRLDATA	Port B Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port B will be detected.
DDPC_CTRLDATA	Port C Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port C will be detected.

Title: **KBL(1/16):DDI/EDP**

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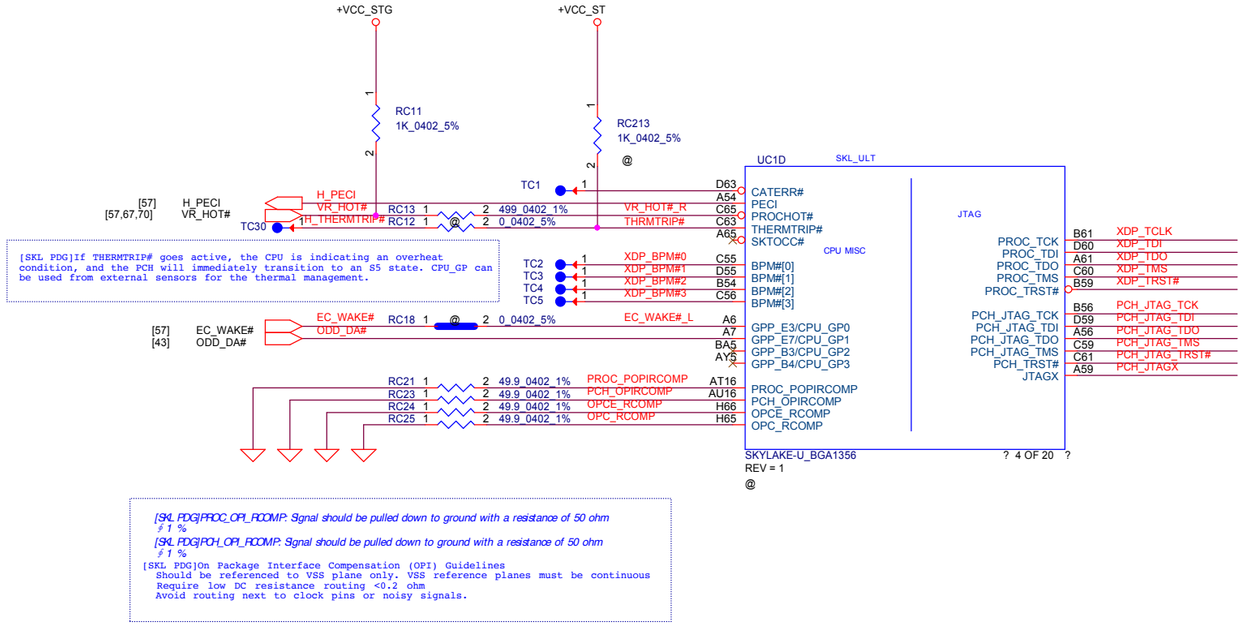

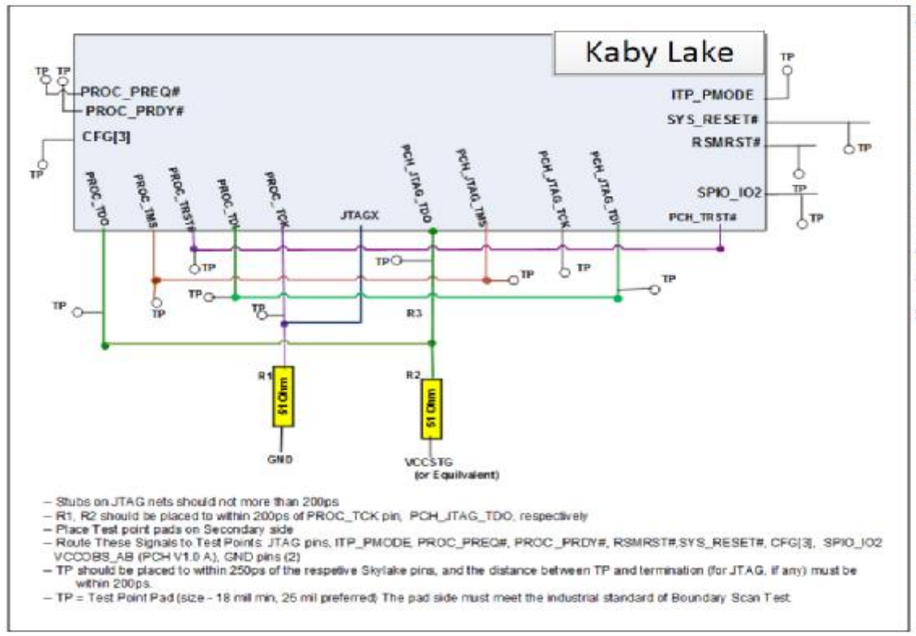

Figure 44-6. Connector Less Routing Topology

XDP_TCLK RC29 1 DCI@ 2 0_0402_5% PCH_JTAGX
XDP_TDI RC30 1 DCI@ 2 0_0402_5% PCH_JTAG_TDI
XDP_TDO RC31 1 DCI@ 2 0_0402_5% PCH_JTAG_TDO
XDP_TMS RC32 1 DCI@ 2 0_0402_5% PCH_JTAG_TMS
XDP_TRST# RC33 1 DCI@ 2 0_0402_5% PCH_JTAG_TRST#

Close to UC1

Termination option

XDP_TCLK

PROC_TCK Termination:
51 ohm +/- 5% pull down to GNG (Ground)
Placed to within 200ps (1100 mil) or PROC_TCK pin

PCH_JTAG_TDO

PCH_JTAG_TDO Termination:
51ohm +/- 5% pull up to VccSTG or equivalent.
Placed to within 200ps (1100 mil) or PCH_JTAG_TDO pin

Title: KBL(2/16):MISC/JTAG

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TABLE

	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
	BA59	DDR0_DQ[30]	DDR0_DQ[46]
	AY59	DDR0_DQ[31]	DDR0_DQ[47]
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA25	DDR0_DQ[62]	DDR1_DQ[46]
	BB25	DDR0_DQ[63]	DDR1_DQ[47]

TABLE

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

TABLE

Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

[22] DDR_A_D[63..0]

UC1B — SKL_ULT

DDR_A_D0 AL71 — DDR0_DQ[0]
DDR_A_D1 AL68 — DDR0_DQ[1]
DDR_A_D2 AN68 — DDR0_DQ[2]
DDR_A_D3 AN69 — DDR0_DQ[3]
DDR_A_D4 AL70 — DDR0_DQ[4]
DDR_A_D5 AL69 — DDR0_DQ[5]
DDR_A_D6 AN70 — DDR0_DQ[6]
DDR_A_D7 AN71 — DDR0_DQ[7]
DDR_A_D8 AR70 — DDR0_DQ[8]
DDR_A_D9 AR68 — DDR0_DQ[9]
DDR_A_D10 AU71 — DDR0_DQ[10]
DDR_A_D11 AU68 — DDR0_DQ[11]
DDR_A_D12 AR71 — DDR0_DQ[12]
DDR_A_D13 AR69 — DDR0_DQ[13]
DDR_A_D14 AU70 — DDR0_DQ[14]
DDR_A_D15 AU69 — DDR0_DQ[15]
DDR_A_D16 BB65 — DDR0_DQ[16]/DDR0_DQ[32]
DDR_A_D17 AW65 — DDR0_DQ[17]/DDR0_DQ[33]
DDR_A_D18 AW63 — DDR0_DQ[18]/DDR0_DQ[34]
DDR_A_D19 AY63 — DDR0_DQ[19]/DDR0_DQ[35]
DDR_A_D20 BA65 — DDR0_DQ[20]/DDR0_DQ[36]
DDR_A_D21 AY65 — DDR0_DQ[21]/DDR0_DQ[37]
DDR_A_D22 BA63 — DDR0_DQ[22]/DDR0_DQ[38]
DDR_A_D23 BB63 — DDR0_DQ[23]/DDR0_DQ[39]
DDR_A_D24 BA61 — DDR0_DQ[24]/DDR0_DQ[40]
DDR_A_D25 AW61 — DDR0_DQ[25]/DDR0_DQ[41]
DDR_A_D26 BB59 — DDR0_DQ[26]/DDR0_DQ[42]
DDR_A_D27 AW59 — DDR0_DQ[27]/DDR0_DQ[43]
DDR_A_D28 BB61 — DDR0_DQ[28]/DDR0_DQ[44]
DDR_A_D29 AY61 — DDR0_DQ[29]/DDR0_DQ[45]
DDR_A_D30 BA59 — DDR0_DQ[30]/DDR0_DQ[46]
DDR_A_D31 AY59 — DDR0_DQ[31]/DDR0_DQ[47]
DDR_A_D32 AY39 — DDR0_DQ[32]/DDR1_DQ[0]
DDR_A_D33 AW39 — DDR0_DQ[33]/DDR1_DQ[1]
DDR_A_D34 AY37 — DDR0_DQ[34]/DDR1_DQ[2]
DDR_A_D35 AW37 — DDR0_DQ[35]/DDR1_DQ[3]
DDR_A_D36 BB39 — DDR0_DQ[36]/DDR1_DQ[4]
DDR_A_D37 BA39 — DDR0_DQ[37]/DDR1_DQ[5]
DDR_A_D38 BA37 — DDR0_DQ[38]/DDR1_DQ[6]
DDR_A_D39 BB37 — DDR0_DQ[39]/DDR1_DQ[7]
DDR_A_D40 AY35 — DDR0_DQ[40]/DDR1_DQ[8]
DDR_A_D41 AW35 — DDR0_DQ[41]/DDR1_DQ[9]
DDR_A_D42 AY33 — DDR0_DQ[42]/DDR1_DQ[10]
DDR_A_D43 AW33 — DDR0_DQ[43]/DDR1_DQ[11]
DDR_A_D44 BB35 — DDR0_DQ[44]/DDR1_DQ[12]
DDR_A_D45 BA35 — DDR0_DQ[45]/DDR1_DQ[13]
DDR_A_D46 BA33 — DDR0_DQ[46]/DDR1_DQ[14]
DDR_A_D47 BB33 — DDR0_DQ[47]/DDR1_DQ[15]
DDR_A_D48 AY31 — DDR0_DQ[48]/DDR1_DQ[32]
DDR_A_D49 AW31 — DDR0_DQ[49]/DDR1_DQ[33]
DDR_A_D50 AY29 — DDR0_DQ[50]/DDR1_DQ[34]
DDR_A_D51 AW29 — DDR0_DQ[51]/DDR1_DQ[35]
DDR_A_D52 BB31 — DDR0_DQ[52]/DDR1_DQ[36]
DDR_A_D53 BA31 — DDR0_DQ[53]/DDR1_DQ[37]
DDR_A_D54 BA29 — DDR0_DQ[54]/DDR1_DQ[38]
DDR_A_D55 BB29 — DDR0_DQ[55]/DDR1_DQ[39]
DDR_A_D56 AY27 — DDR0_DQ[56]/DDR1_DQ[40]
DDR_A_D57 AW27 — DDR0_DQ[57]/DDR1_DQ[41]
DDR_A_D58 AY25 — DDR0_DQ[58]/DDR1_DQ[42]
DDR_A_D59 AW25 — DDR0_DQ[59]/DDR1_DQ[43]
DDR_A_D60 BB27 — DDR0_DQ[60]/DDR1_DQ[44]
DDR_A_D61 BA27 — DDR0_DQ[61]/DDR1_DQ[45]
DDR_A_D62 BA25 — DDR0_DQ[62]/DDR1_DQ[46]
DDR_A_D63 BB25 — DDR0_DQ[63]/DDR1_DQ[47]

DDR CH - A

SKYLAKE-U_BGA1356
REV = 1
@

2 OF 20 ?

DDR0_CKN[0] AU53 — DDR_A_DDRCLK0_1866M# — DDR_A_DDRCLK0_1866M# [22]
DDR0_CKP[0] AT53 — DDR_A_DDRCLK0_1866M — DDR_A_DDRCLK0_1866M [22]
DDR0_CKN[1] AU55 — DDR_A_DDRCLK1_1866M# — DDR_A_DDRCLK1_1866M# [22]
DDR0_CKP[1] AT55 — DDR_A_DDRCLK1_1866M — DDR_A_DDRCLK1_1866M [22]

DDR0_CKE[0] BA56 — DDR_A_CKE0 — DDR_A_CKE0 [22]
DDR0_CKE[1] BB56 — DDR_A_CKE1 — DDR_A_CKE1 [22]
DDR0_CKE[2] AW56
DDR0_CKE[3] AY56

DDR0_CS#[0] AU45 — DDR_A_CS0# — DDR_A_CS0# [22]
DDR0_CS#[1] AU43 — DDR_A_CS1# — DDR_A_CS1# [22]
DDR0_ODT[0] AT45 — DDR_A_ODT0 — DDR_A_ODT0 [22]
DDR0_ODT[1] AT43 — DDR_A_ODT1 — DDR_A_ODT1 [22]

DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5] BA51 — DDR_A_MA5
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9] BB54 — DDR_A_MA9
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6] BA52 — DDR_A_MA6
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8] AY52 — DDR_A_MA8
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7] AW52 — DDR_A_MA7
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0] AY55 — DDR_A_BG0
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12] AW54 — DDR_A_MA12 — DDR_A_BG0 [22]
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11] BA54 — DDR_A_MA11
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT# BA55 — DDR_A_ACT_N — DDR_A_ACT_N [22]
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1] AY54 — DDR_A_BG1 — DDR_A_BG1 [22]

DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13] AU46 — DDR_A_MA13
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15] AU48 — DDR_A_MA15
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14] AT46 — DDR_A_MA14
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16] AU50 — DDR_A_MA16
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0] AU52 — DDR_A_BA0 — DDR_A_BA0 [22]
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2] AY51 — DDR_A_MA2
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1] AT48 — DDR_A_BA1 — DDR_A_BA1 [22]
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10] AT50 — DDR_A_MA10
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1] BB50 — DDR_A_MA1
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0] AY50 — DDR_A_MA0
DDR0_MA[3] BA50 — DDR_A_MA3
DDR0_MA[4] BB52 — DDR_A_MA4

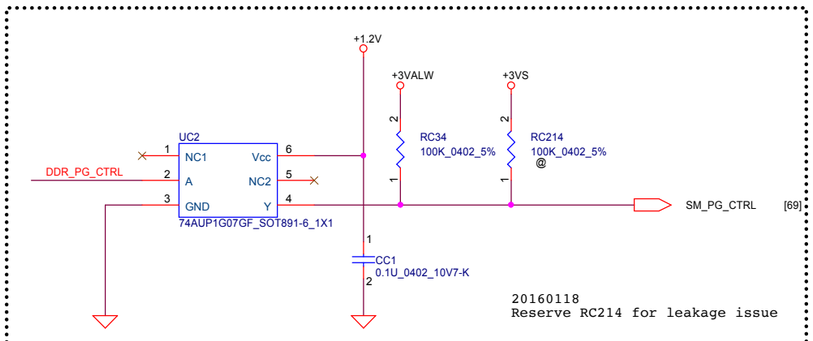
DDR0_DQSN[0] AM70 — DDR_A_DQS#0
DDR0_DQSP[0] AM69 — DDR_A_DQS0
DDR0_DQSN[1] AT69 — DDR_A_DQS#1
DDR0_DQSP[1] AT70 — DDR_A_DQS1
DDR0_DQSN[2]/DDR0_DQSN[4] BA64 — DDR_A_DQS#2
DDR0_DQSP[2]/DDR0_DQSP[4] AY64 — DDR_A_DQS2
DDR0_DQSN[3]/DDR0_DQSN[5] AY60 — DDR_A_DQS#3
DDR0_DQSP[3]/DDR0_DQSP[5] BA60 — DDR_A_DQS3
DDR0_DQSN[4]/DDR1_DQSN[0] BA38 — DDR_A_DQS#4
DDR0_DQSP[4]/DDR1_DQSP[0] AY38 — DDR_A_DQS4
DDR0_DQSN[5]/DDR1_DQSN[1] AY34 — DDR_A_DQS#5
DDR0_DQSP[5]/DDR1_DQSP[1] BA34 — DDR_A_DQS5
DDR0_DQSN[6]/DDR1_DQSN[4] BA30 — DDR_A_DQS#6
DDR0_DQSP[6]/DDR1_DQSP[4] AY30 — DDR_A_DQS6
DDR0_DQSN[7]/DDR1_DQSN[5] AY26 — DDR_A_DQS#7
DDR0_DQSP[7]/DDR1_DQSP[5] BA26 — DDR_A_DQS7

DDR0_ALERT# AW50 — DDR_A_ALERT_N — DDR_A_ALERT_N [22]
DDR0_PAR AT52 — DDR_A_PARITY — DDR_A_PARITY [22]

DDR_VREF_CA AY67 — DDR4_VREF_CA_CPU_A — DDR4_VREF_CA_CPU_A [22]
DDR0_VREF_DQ AY68 — DDR4_VREF_DQ_CPU_A — TC31 — DDR4_VREF_DQ_CPU_B [23]
DDR1_VREF_DQ BA67 — DDR4_VREF_DQ_CPU_B

DDR_VTT_CNTL AW67 — DDR_PG_CTRL

DDR_A_MA0 … DDR_A_MA16 — DDR_A_MA[0..16] [22]
DDR_A_DQS#0 … DDR_A_DQS#7 — DDR_A_DQS#[0..7] [22]
DDR_A_DQS0 … DDR_A_DQS7 — DDR_A_DQS[0..7] [22]



Security Classification	LC Future Center Secret Data		
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TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF85	DDR1_DQ[0]	DDR0_DQ[16]
	AF84	DDR1_DQ[1]	DDR0_DQ[17]
	AK85	DDR1_DQ[2]	DDR0_DQ[18]
	AK84	DDR1_DQ[3]	DDR0_DQ[19]
	AF86	DDR1_DQ[4]	DDR0_DQ[20]
	AF87	DDR1_DQ[6]	DDR0_DQ[21]
	AK87	DDR1_DQ[6]	DDR0_DQ[22]
	AK86	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF88	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH88	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF89	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH89	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT86	DDR1_DQ[16]	DDR0_DQ[48]
	AU86	DDR1_DQ[17]	DDR0_DQ[49]
	AP85	DDR1_DQ[18]	DDR0_DQ[50]
	AN85	DDR1_DQ[19]	DDR0_DQ[51]
	AN86	DDR1_DQ[20]	DDR0_DQ[52]
	AP86	DDR1_DQ[21]	DDR0_DQ[53]
	AT85	DDR1_DQ[22]	DDR0_DQ[54]
	AU85	DDR1_DQ[23]	DDR0_DQ[55]
	AT81	DDR1_DQ[24]	DDR0_DQ[56]
	AU81	DDR1_DQ[25]	DDR0_DQ[57]
	AP80	DDR1_DQ[26]	DDR0_DQ[58]
	AN80	DDR1_DQ[27]	DDR0_DQ[59]
	AN81	DDR1_DQ[28]	DDR0_DQ[60]
	AP81	DDR1_DQ[29]	DDR0_DQ[61]
	AT80	DDR1_DQ[30]	DDR0_DQ[62]
	AU80	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AT37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AU33	DDR1_DQ[40]	DDR1_DQ[24]
	AT33	DDR1_DQ[41]	DDR1_DQ[25]
	AR33	DDR1_DQ[42]	DDR1_DQ[26]
	AP33	DDR1_DQ[43]	DDR1_DQ[27]
	AR30	DDR1_DQ[44]	DDR1_DQ[28]
	AP30	DDR1_DQ[45]	DDR1_DQ[29]
	AU30	DDR1_DQ[46]	DDR1_DQ[30]
	AT30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY45	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

[23] DDR_B_D[0..63]

UC1C

SKL_ULT

DDR_B_D0 AF65
DDR_B_D1 AF64
DDR_B_D2 AK65
DDR_B_D3 AK64
DDR_B_D4 AF66
DDR_B_D5 AF67
DDR_B_D6 AK67
DDR_B_D7 AK66
DDR_B_D8 AF70
DDR_B_D9 AF68
DDR_B_D10 AH71
DDR_B_D11 AH68
DDR_B_D12 AF71
DDR_B_D13 AF69
DDR_B_D14 AH70
DDR_B_D15 AH69
DDR_B_D16 AT66
DDR_B_D17 AU66
DDR_B_D18 AP65
DDR_B_D19 AN65
DDR_B_D20 AN66
DDR_B_D21 AP66
DDR_B_D22 AT65
DDR_B_D23 AU65
DDR_B_D24 AT61
DDR_B_D25 AU61
DDR_B_D26 AP60
DDR_B_D27 AN60
DDR_B_D28 AN61
DDR_B_D29 AP61
DDR_B_D30 AT60
DDR_B_D31 AU60
DDR_B_D32 AU40
DDR_B_D33 AT40
DDR_B_D34 AT37
DDR_B_D35 AU37
DDR_B_D36 AR40
DDR_B_D37 AP40
DDR_B_D38 AP37
DDR_B_D39 AR37
DDR_B_D40 AT33
DDR_B_D41 AU33
DDR_B_D42 AU30
DDR_B_D43 AT30
DDR_B_D44 AR33
DDR_B_D45 AP33
DDR_B_D46 AR30
DDR_B_D47 AP30
DDR_B_D48 AU27
DDR_B_D49 AT27
DDR_B_D50 AT25
DDR_B_D51 AU25
DDR_B_D52 AP27
DDR_B_D53 AN27
DDR_B_D54 AN25
DDR_B_D55 AP25
DDR_B_D56 AT22
DDR_B_D57 AU22
DDR_B_D58 AU21
DDR_B_D59 AT21
DDR_B_D60 AN22
DDR_B_D61 AP22
DDR_B_D62 AP21
DDR_B_D63 AN21

DDR1_DQ[0]/DDR0_DQ[16]
DDR1_DQ[1]/DDR0_DQ[17]
DDR1_DQ[2]/DDR0_DQ[18]
DDR1_DQ[3]/DDR0_DQ[19]
DDR1_DQ[4]/DDR0_DQ[20]
DDR1_DQ[5]/DDR0_DQ[21]
DDR1_DQ[6]/DDR0_DQ[22]
DDR1_DQ[7]/DDR0_DQ[23]
DDR1_DQ[8]/DDR0_DQ[24]
DDR1_DQ[9]/DDR0_DQ[25]
DDR1_DQ[10]/DDR0_DQ[26]
DDR1_DQ[11]/DDR0_DQ[27]
DDR1_DQ[12]/DDR0_DQ[28]
DDR1_DQ[13]/DDR0_DQ[29]
DDR1_DQ[14]/DDR0_DQ[30]
DDR1_DQ[15]/DDR0_DQ[31]
DDR1_DQ[16]/DDR0_DQ[48]
DDR1_DQ[17]/DDR0_DQ[49]
DDR1_DQ[18]/DDR0_DQ[50]
DDR1_DQ[19]/DDR0_DQ[51]
DDR1_DQ[20]/DDR0_DQ[52]
DDR1_DQ[21]/DDR0_DQ[53]
DDR1_DQ[22]/DDR0_DQ[54]
DDR1_DQ[23]/DDR0_DQ[55]
DDR1_DQ[24]/DDR0_DQ[56]
DDR1_DQ[25]/DDR0_DQ[57]
DDR1_DQ[26]/DDR0_DQ[58]
DDR1_DQ[27]/DDR0_DQ[59]
DDR1_DQ[28]/DDR0_DQ[60]
DDR1_DQ[29]/DDR0_DQ[61]
DDR1_DQ[30]/DDR0_DQ[62]
DDR1_DQ[31]/DDR0_DQ[63]
DDR1_DQ[32]/DDR1_DQ[16]
DDR1_DQ[33]/DDR1_DQ[17]
DDR1_DQ[34]/DDR1_DQ[18]
DDR1_DQ[35]/DDR1_DQ[19]
DDR1_DQ[36]/DDR1_DQ[20]
DDR1_DQ[37]/DDR1_DQ[21]
DDR1_DQ[38]/DDR1_DQ[22]
DDR1_DQ[39]/DDR1_DQ[23]
DDR1_DQ[40]/DDR1_DQ[24]
DDR1_DQ[41]/DDR1_DQ[25]
DDR1_DQ[42]/DDR1_DQ[26]
DDR1_DQ[43]/DDR1_DQ[27]
DDR1_DQ[44]/DDR1_DQ[28]
DDR1_DQ[45]/DDR1_DQ[29]
DDR1_DQ[46]/DDR1_DQ[30]
DDR1_DQ[47]/DDR1_DQ[31]
DDR1_DQ[48]
DDR1_DQ[49]
DDR1_DQ[50]
DDR1_DQ[51]
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DDR1_DQ[55]
DDR1_DQ[56]
DDR1_DQ[57]
DDR1_DQ[58]
DDR1_DQ[59]
DDR1_DQ[60]
DDR1_DQ[61]
DDR1_DQ[62]
DDR1_DQ[63]

DDR CH - B

SKYLAKE-U_BGA1356
REV = 1
@

3 OF 20 ?

DDR1_CKN[0] AN45
DDR1_CKN[1] AN46
DDR1_CKP[0] AP45
DDR1_CKP[1] AP46
DDR1_CKE[0] AN56
DDR1_CKE[1] AP55
DDR1_CKE[2] AN55
DDR1_CKE[3] AP53
DDR1_CS#[0] BB42
DDR1_CS#[1] AY42
DDR1_ODT[0] BA42
DDR1_ODT[1] AW42

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5] AY48
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9] AP50
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6] BA48
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8] BB48
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7] AP48
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0] AP52
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12] AN50
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11] AN48
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT# AN53
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1] AN52

DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13] BA43
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15] AY43
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14] AY44
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16] AW44
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0] BB44
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2] AY47
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1] BA44
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10] AW46
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1] AY46
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0] BA46
DDR1_MA[3] BB46
DDR1_MA[4] BA47

DDR1_DQSN[0]/DDR0_DQSN[2] AH66
DDR1_DQSP[0]/DDR0_DQSP[2] AH65
DDR1_DQSN[1]/DDR0_DQSN[3] AG69
DDR1_DQSP[1]/DDR0_DQSP[3] AG70
DDR1_DQSN[2]/DDR0_DQSN[6] AR66
DDR1_DQSP[2]/DDR0_DQSP[6] AR65
DDR1_DQSN[3]/DDR0_DQSN[7] AR61
DDR1_DQSP[3]/DDR0_DQSP[7] AR60
DDR1_DQSN[4]/DDR1_DQSN[2] AT38
DDR1_DQSP[4]/DDR1_DQSP[2] AR38
DDR1_DQSN[5]/DDR1_DQSN[3] AT32
DDR1_DQSP[5]/DDR1_DQSN[3] AR32
DDR1_DQSN[6] AR25
DDR1_DQSP[6] AR27
DDR1_DQSN[7] AR22
DDR1_DQSP[7] AR21

DDR1_ALERT# AN43
DDR1_PAR AP43
DRAM_RESET# AT13
DDR_RCOMP[0] AR18
DDR_RCOMP[1] AT18
DDR_RCOMP[2] AU18

DDR_B_DDRCLK0_1866M# → DDR_B_DDRCLK0_1866M# [23]
DDR_B_DDRCLK1_1866M# → DDR_B_DDRCLK1_1866M# [23]
DDR_B_DDRCLK0_1866M → DDR_B_DDRCLK0_1866M [23]
DDR_B_DDRCLK1_1866M → DDR_B_DDRCLK1_1866M [23]
DDR_B_CKE0 → DDR_B_CKE0 [23]
DDR_B_CKE1 → DDR_B_CKE1 [23]
DDR_B_CS0# → DDR_B_CS0# [23]
DDR_B_CS1# → DDR_B_CS1# [23]
DDR_B_ODT0 → DDR_B_ODT0 [23]
DDR_B_ODT1 → DDR_B_ODT1 [23]

DDR_B_MA5 AY48
DDR_B_MA9 AP50
DDR_B_MA6 BA48
DDR_B_MA8 BB48
DDR_B_MA7 AP48
DDR_B_BG0 AP52 → DDR_B_BG0 [23]
DDR_B_MA12 AN50
DDR_B_MA11 AN48
DDR_B_ACT_N AN53 → DDR_B_ACT_N [23]
DDR_B_BG1 AN52 → DDR_B_BG1 [23]
DDR_B_MA13 BA43
DDR_B_MA15 AY43
DDR_B_MA14 AY44
DDR_B_MA16 AW44
DDR_B_BA0 BB44 → DDR_B_BA0 [23]
DDR_B_MA2 AY47
DDR_B_BA1 BA44 → DDR_B_BA1 [23]
DDR_B_MA10 AW46
DDR_B_MA1 AY46
DDR_B_MA0 BA46
DDR_B_MA3 BB46
DDR_B_MA4 BA47

DDR_B_DQS#0 AH66
DDR_B_DQS0 AH65
DDR_B_DQS#1 AG69
DDR_B_DQS1 AG70
DDR_B_DQS#2 AR66
DDR_B_DQS2 AR65
DDR_B_DQS#3 AR61
DDR_B_DQS3 AR60
DDR_B_DQS#4 AT38
DDR_B_DQS4 AR38
DDR_B_DQS#5 AT32
DDR_B_DQS5 AR32
DDR_B_DQS#6 AR25
DDR_B_DQS6 AR27
DDR_B_DQS#7 AR22
DDR_B_DQS7 AR21

DDR_B_ALERT_N AN43 → DDR_B_ALERT_N [23]
DDR_B_PARITY AP43 → DDR_B_PARITY [23]
DDR4_DRAMRST_N AT13
SM_RCOMP0 AR18 — RC36 1 — 2 121_0402_1%
SM_RCOMP1 AT18 — RC38 1 — 2 80.6_0402_1%
SM_RCOMP2 AU18 — RC39 1 — 2 100_0402_1%

[KBL PDG]for DDR4 COMPENSATION
DDR_RCOMP[0] Pull down 121 ohm resistor
DDR_RCOMP[1] Pull down 80.6 ohm resistor
DDR_RCOMP[2] Pull down 100 ohm resistor

DDR_B_MA0
DDR_B_MA1
DDR_B_MA2
DDR_B_MA3
DDR_B_MA4
DDR_B_MA5
DDR_B_MA6
DDR_B_MA7
DDR_B_MA8
DDR_B_MA9
DDR_B_MA10
DDR_B_MA11
DDR_B_MA12
DDR_B_MA13
DDR_B_MA14
DDR_B_MA15
DDR_B_MA16
→ DDR_B_MA[0..16] [23]

DDR_B_DQS#0
DDR_B_DQS#1
DDR_B_DQS#2
DDR_B_DQS#3
DDR_B_DQS#4
DDR_B_DQS#5
DDR_B_DQS#6
DDR_B_DQS#7
→ DDR_B_DQS#[0..7] [23]

DDR_B_DQS0
DDR_B_DQS1
DDR_B_DQS2
DDR_B_DQS3
DDR_B_DQS4
DDR_B_DQS5
DDR_B_DQS6
DDR_B_DQS7
→ DDR_B_DQS[0..7] [23]

+1.2V
RC35 2 — 1 470_0402_5%
DDR4_DRAMRST_N — RC37 1 — 2 0_0402_5% → DDR4_DRAMRST# [22,23]

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

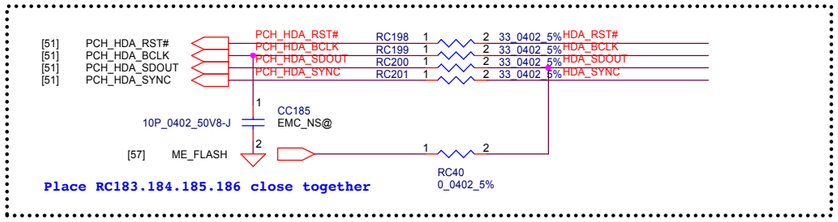
Title: KBL(4/16):DDR4 CH.B

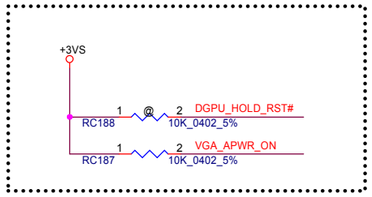
LCFC

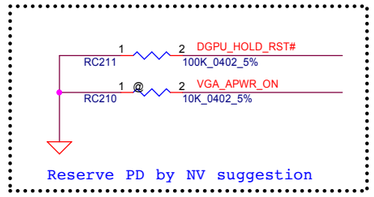
Size: Custom | Document Number: SKYWALKER | Rev: 2.0

Date: Thursday, August 25, 2016 | Sheet 8 of 82

[KBL PDG]Manufacturing Mode Jumper
1. If strap is sampled low, the security measures defined in
the Flash Descriptor will be in effect (default)
2. If sampled high, the Flash Descriptor Security will be overridden.

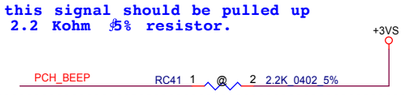




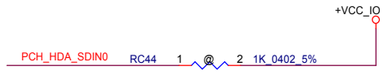


Note:
SPKR (PC_BEEP) has an integrated weak pull-down resistor (20 K ohm nominal) to disable Top-Block Sway by default.

To enable Top-Block Swap, this signal should be pulled up to V3.3S through a 1k to 2.2 Kohm ±5% resistor.

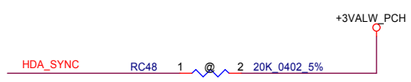


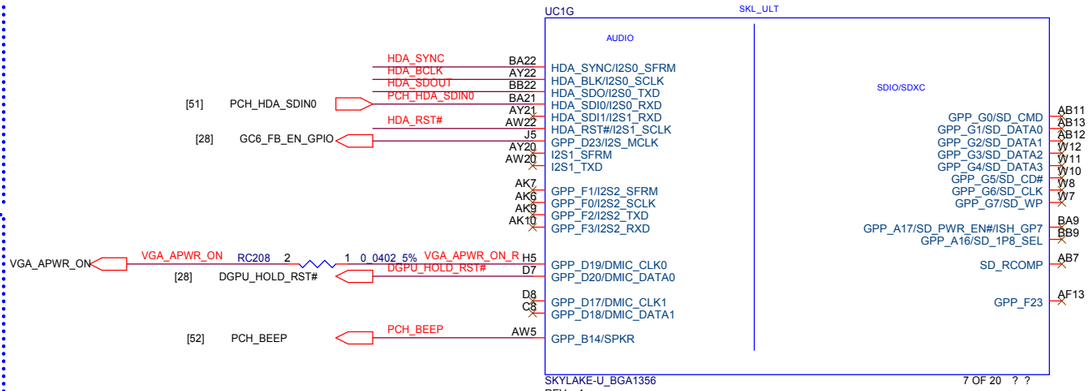
Note:
Internal PD 20K



Note:
HDA_SDO should only be asserted high via external pull-up to 3.3A rail in manufacturing/debug environments ONLY.

Note:
Internal PD 20K





[SKL PDG] internal SD Card

Not support internal SD card. Remove SD_RCOMP

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(5/16):HDA/SDIO

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

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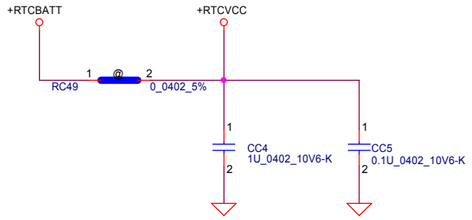
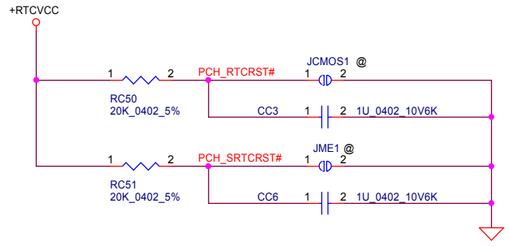
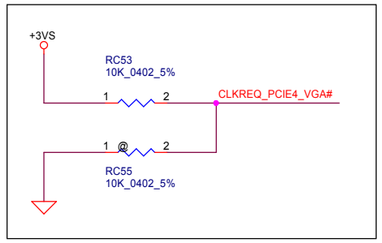
RTC External Circuit

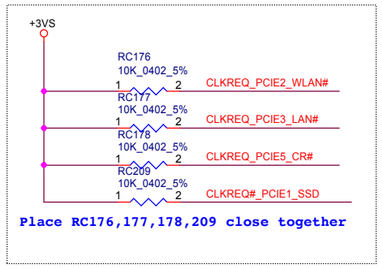
+RTCBATT, +RTCVCC
Trace width = 20mils



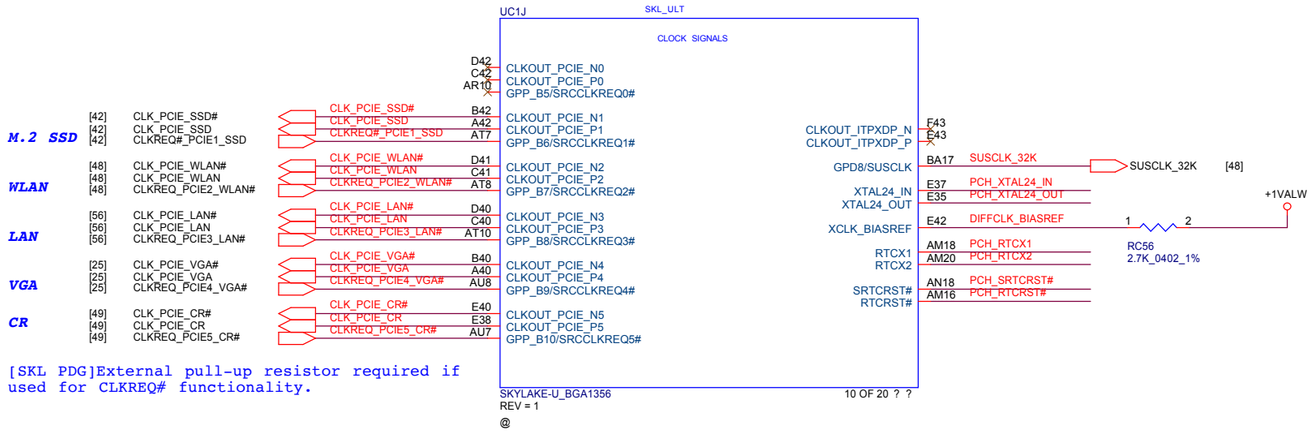
JCMOS, JME Setting, Need Under DDR Door





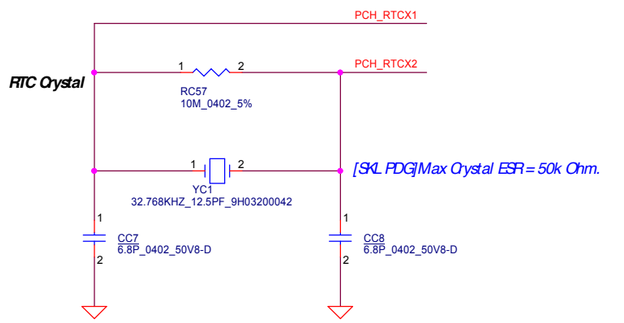


Place RC176,177,178,209 close together



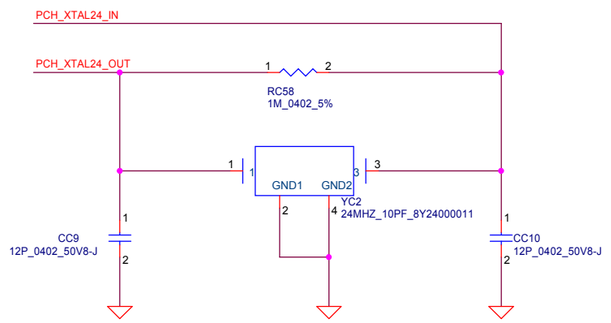
[SKL PDG]External pull-up resistor required if used for CLKREQ# functionality.

[SKL PDG]
1.Space > 15mils
2.No trace under crystal
3.Place on oppsosit side of MCP for temp inf l uence
4.The exact capacitor values forC1 and C2 must be based on the crystal maker recommendat i ons
Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.



20160127
Change CC7/CC8 to 6.8p by vender suggestion

[SKL PDG]
1.A 24 MHz crystal with crystal frequency tolerance and stability of +/-30 ppm
2.Two External Load Capacitors (Ce1 and Ce2)
3.A 1-Mohm bias resistor (Rf)



Security Classification	LC Future Center Secret Data		
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Title: **KBL(6/16):CLOCK SIGNALS**

Size	Document Number	Rev
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Functional Strap Definitions

L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
*H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).Support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

+3VALW_PCH
SMBALERT# — 1 — RC59 — 2 — 1K_0402_5%

GPP_C2, Internal PD 20K

JTAG ODT

SPI0_MOSI

+3VALW_PCH
SPI_SI — 1 — @ — RC62 — 2 — 8.2K_0402_5%

+3VALW_PCH
SPI_SO — 1 — @ — RC65 — 2 — 8.2K_0402_5%

GPP_C5, Internal PD 20K

*L: LPC
H: eSPI

+3VALW_PCH
SML0ALERT# — 1 — @ — RC67 — 2 — 1K_0402_5%

+3VS
Place RC179,180,181 close together

RC1791 2 10K_0402_5% SERIRQ
RC1801 2 10K_0402_5% EC_SCI#
RC1811 2 10K_0402_5% KBRST#
RC72 1 2 4.7K_0402_5% CP_SMB_CLK
RC76 1 2 4.7K_0402_5% CP_SMB_DAT
RC2121 2 10K_0402_5% GPU_EVENT#

+3VALW_PCH
PCH_SMB_CLK — RC71 1 2 2.2K_0402_1%
PCH_SMB_DATA — RC73 1 2 2.2K_0402_1%
PCH_SML1CLK — RC74 1 2 2.2K_0402_1%
PCH_SML1DATA — RC75 1 2 2.2K_0402_1%

Add RC212 PU by NV suggestion

SML1ALERT# — RC77 1 @ 2 1K_0402_5%

close to CPU

UC1E — SKL_ULT

SPI - FLASH
[21,58] SPI_CLK — SPI_CLK — AV2 — SPI0_CLK
[21,58] SPI_SO — SPI_SO — AW3 — SPI0_MISO
[21,58] SPI_SI — SPI_SI — AV3 — SPI0_MOSI
[21] SPI_IO2 — SPI_IO2 — AW2 — SPI0_IO2
[21] SPI_IO3 — SPI_IO3 — AU4 — SPI0_IO3
[21] SPI_CS0#_8MB — SPI_CS0#_8MB — AU3 — SPI0_CS0#
[21] SPI_CS1#_4MB — SPI_CS1#_4MB — AU2 — SPI0_CS1#
[58] SPI_CS2#_TPM — SPI_CS2#_TPM — AU1 — SPI0_CS2#

SPI - TOUCH
M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

[25] All_GPU_PWRGD — RC107 1 2 0_0402_5% — All_GPU_PWRGD_R
[28] GPU_EVENT# — GPU_EVENT#
[57] EC_SCI# — EC_SCI#

C LINK
[48] CL_CLK_WLAN — G3 CL_CLK
[48] CL_DATA_WLAN — G2 CL_DATA
[48] CL_RST_WLAN# — G1 CL_RST#

[57] KBRST# — KBRST# — AW13 GPP_A0/RCIN#
SERIRQ — AY11 GPP_A6/SERIRQ
CC183 10P_0402_50V8-J [57,58] SERIRQ — EMC_NS@

SKYLAKE-U_BGA1356
REV = 1
@

SMBUS, SMLINK
GPP_C0/SMBCLK — R7 — PCH_SMB_CLK
GPP_C1/SMBDATA — R8 — PCH_SMB_DATA
GPP_C2/SMBALERT# — R10 — SMBALERT#
GPP_C3/SML0CLK — R9
GPP_C4/SML0DATA — W2
GPP_C5/SML0ALERT# — W1 — SML0ALERT#
GPP_C6/SML1CLK — W3 — PCH_SML1CLK
GPP_C7/SML1DATA — V3 — PCH_SML1DATA
GPP_B23/SML1ALERT#/PCHHOT# — AM7 — SML1ALERT#

LPC
GPP_A1/LAD0/ESPI_IO0 — AY13 — LPC_AD0 [57]
GPP_A2/LAD1/ESPI_IO1 — BA13 — LPC_AD1 [57]
GPP_A3/LAD2/ESPI_IO2 — BB13 — LPC_AD2 [57]
GPP_A4/LAD3/ESPI_IO3 — AY12 — LPC_AD3 [57]
GPP_A5/LFRAME#/ESPI_CS# — BA12 — LPC_FRAME# [57]
GPP_A14/SUS_STAT#/ESPI_RESET# — BA11 — SUS_STAT#

GPP_A9/CLKOUT_LPC0/ESPI_CLK — AW9 — PCH_PCI_CLK_R
GPP_A10/CLKOUT_LPC1 — AY9
GPP_A8/CLKRUN# — AW11 — CLKRUN#

5 OF 20 ? ?

RC63 0_0402_5% — 1 @ 2 — 1 — TC7
1 EMC@ 2 — CLK_PCI_EC [57]
RC64 22_0402_5%
CC184 10P_0402_50V8-J — EMC_NS@
RC66 8.2K_0402_5% — +3VS

Close to UC1

DIMM1, DIMM2, Security EEPROM, Click Pad

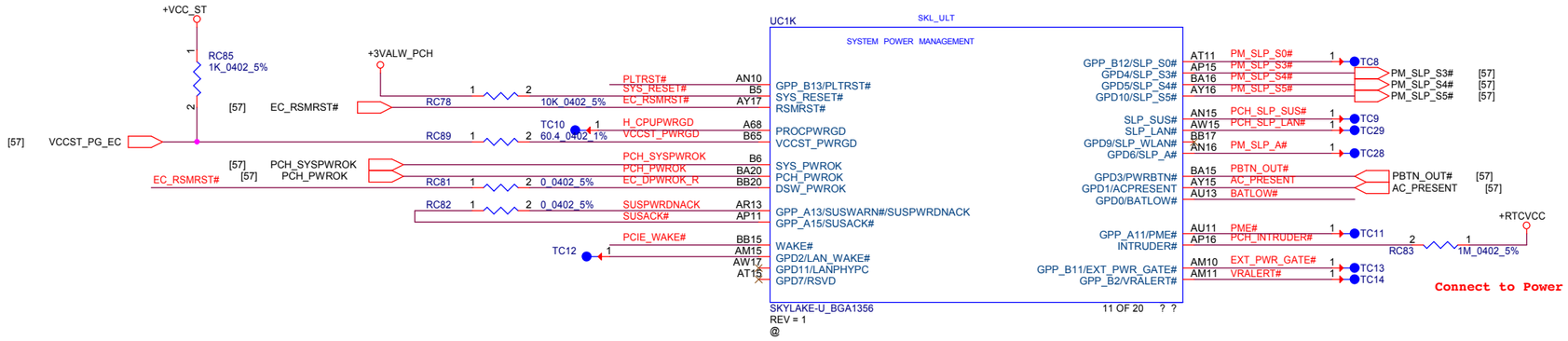
EC,dGPU,Thermal Sensor

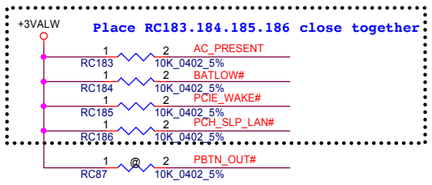
SB00000YS00
2N7002KDWH_SOT363-6
QC1A
PCH_SMB_CLK — 6 — 1 — CP_SMB_CLK [22,23,63]
+3VS — 2
Plan to remove QC1 after SDV
PCH_SMB_DATA — 3 — 4 — CP_SMB_DAT [22,23,63]
QC1B
2N7002KDWH_SOT363-6
SB00000YS00

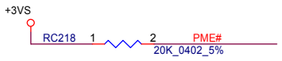
SB00000YS00
2N7002KDWH_SOT363-6
QC2A
+3VS — PCH_SML1CLK — 6 — 1 — EC_SMB_CK3 [28,57,59,62]
2
PCH_SML1DATA — 3 — 4 — EC_SMB_DA3 [28,57,59,62]
QC2B
2N7002KDWH_SOT363-6
SB00000YS00

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

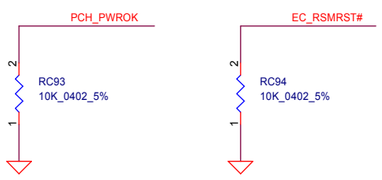
Title: KBL(7/16):LPC/SPI/SMBUS/CL
Size: Custom | Document Number: SKYWALKER | Rev: 2.0
Date: Thursday, August 25, 2016 | Sheet 11 of 82

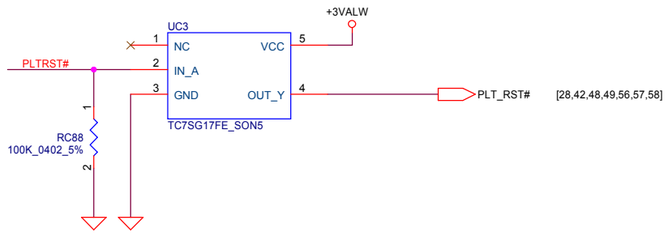






20160408
1.Add RC218 for PME# by BIOS request





Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(8/16):SYSTEM PM

Size	Document Number	Rev
Custom	SKYWALKER	2.0

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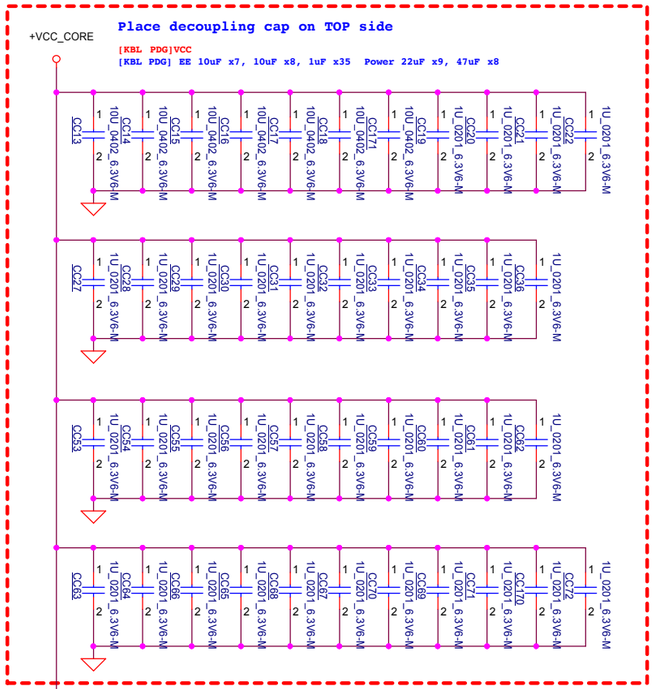
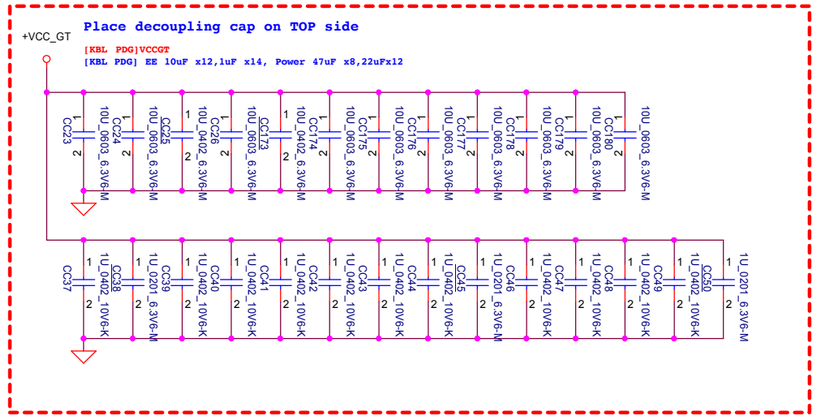


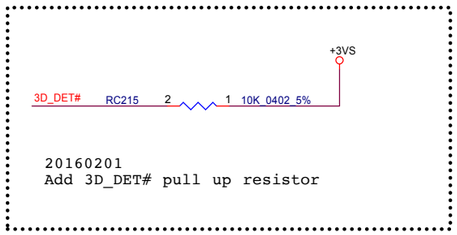


Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KBL(9/16):Decoupling**

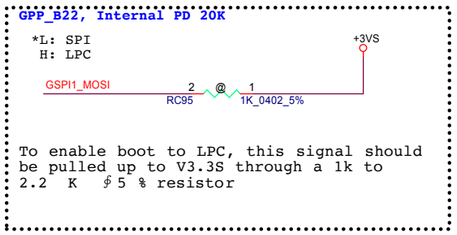
Size	Document Number	Rev
Custom	SKYWALKER	2.0

Date: Thursday, August 25, 2016 Sheet 13 of 82



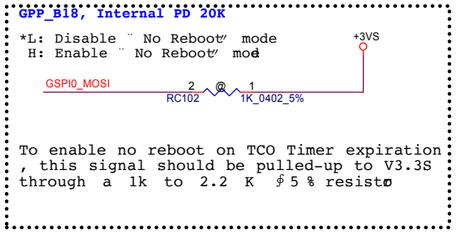
20160201
Add 3D_DET# pull up resistor

GPP_B22, Internal PD 20K



To enable boot to LPC, this signal should be pulled up to V3.3S through a 1k to 2.2 K ±5 % resistor

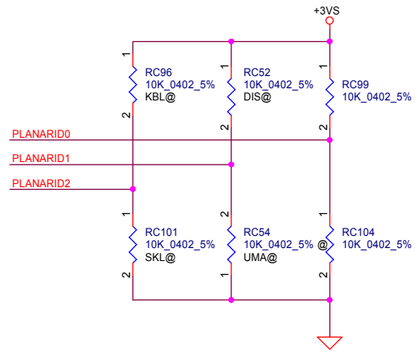
GPP_B18, Internal PD 20K

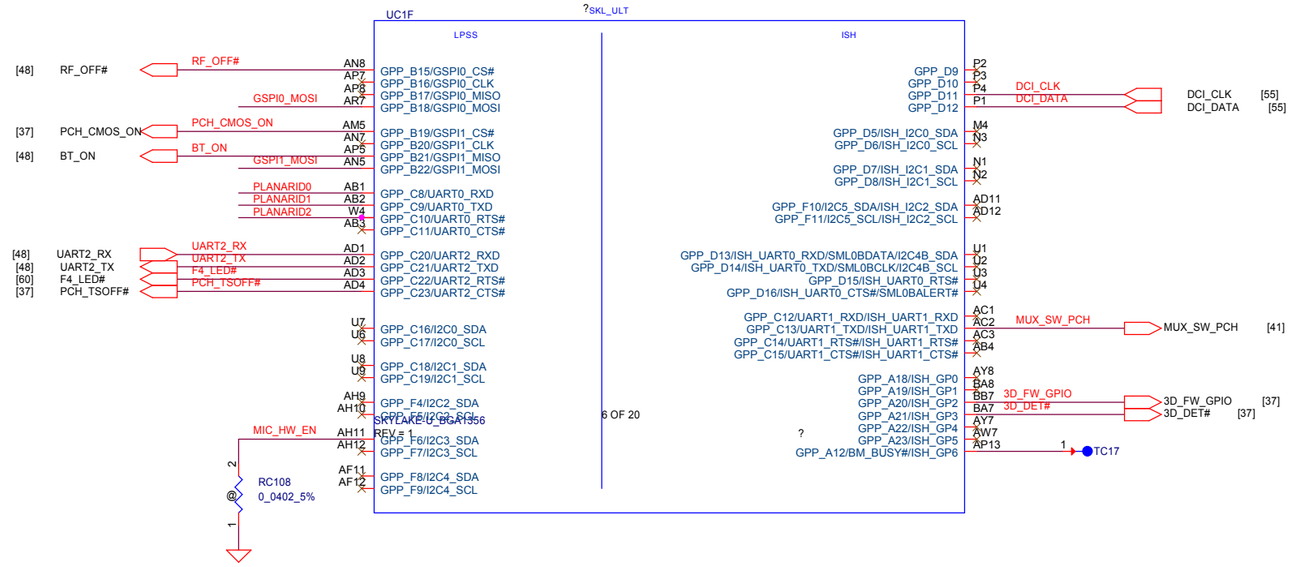


To enable no reboot on TCO Timer expiration, this signal should be pulled-up to V3.3S through a 1k to 2.2 K ±5 % resistor

Project ID

	PLANARID0 (GPP_C8)	PLANARID1 (GPP_C9)	PLANARID2 (GPP_C10)	
L	14"	UMA	Skylake	
H	15"	DIS	Kabylake	



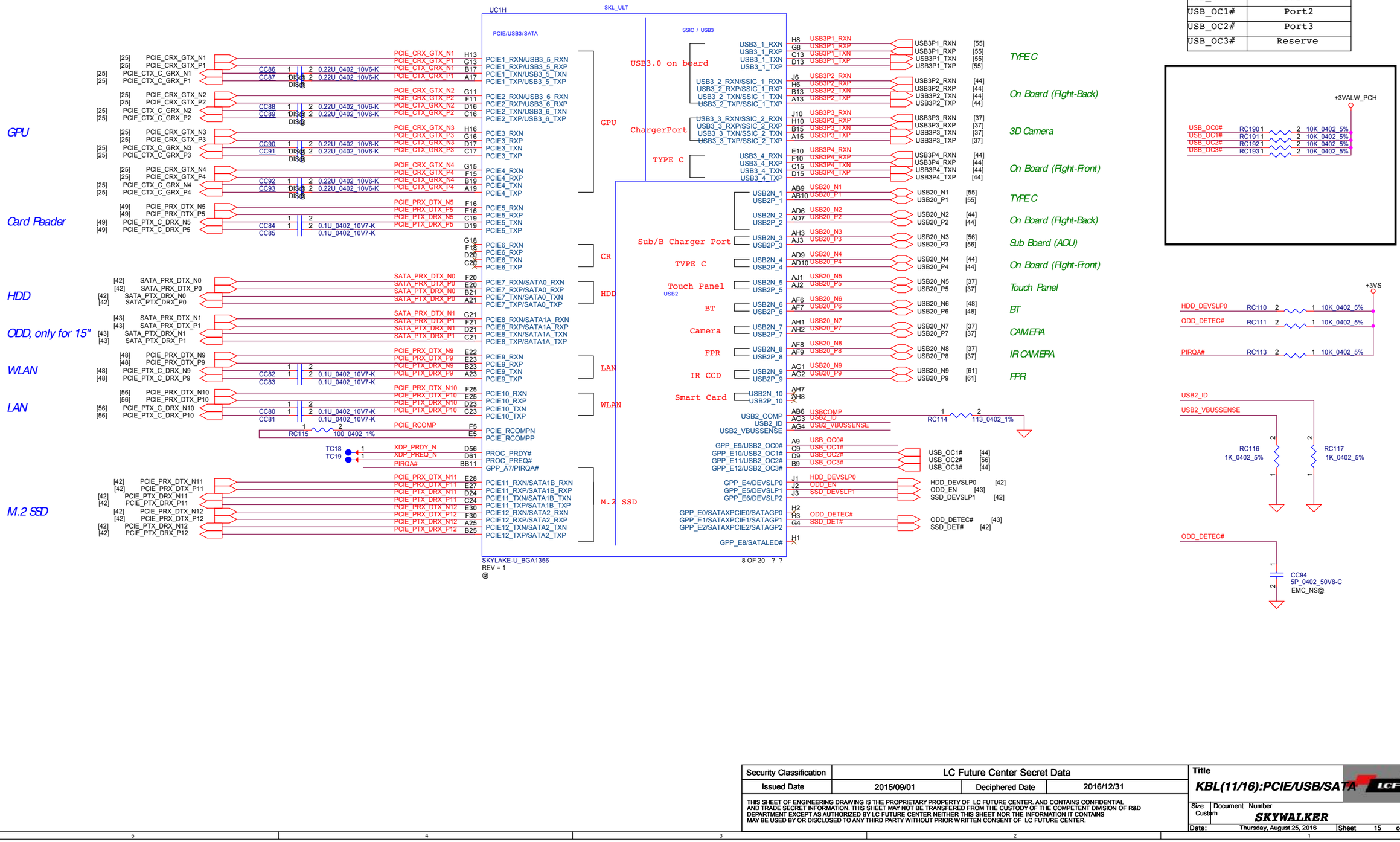


Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(10/16):GPIO/CPU/MISC

Size	Document Number	Rev
Custom	SKYWALKER	2.0

Date: Thursday, August 25, 2016 Sheet 14 of 82



	USB Port Number
USB_OC0#	Port1
USB_OC1#	Port2
USB_OC2#	Port3
USB_OC3#	Reserve

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

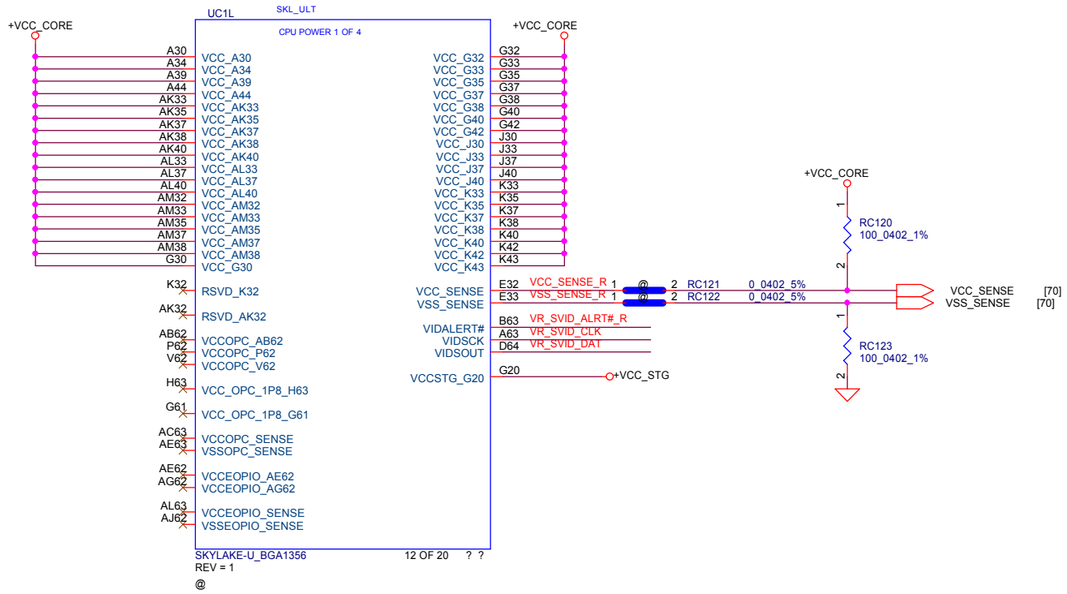
Title: KBL(11/16):PCIE/USB/SATA

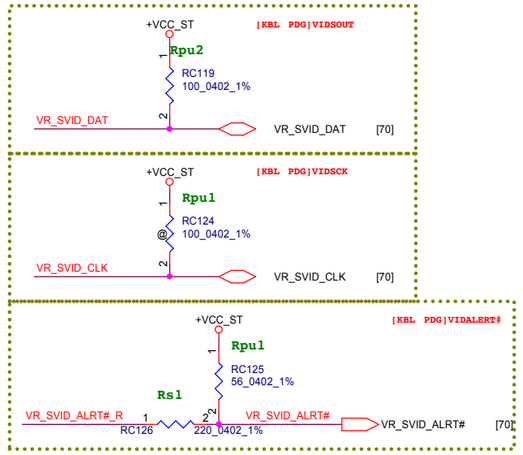
Size: Custom | Document Number: SKYWALKER | Rev: 2.0

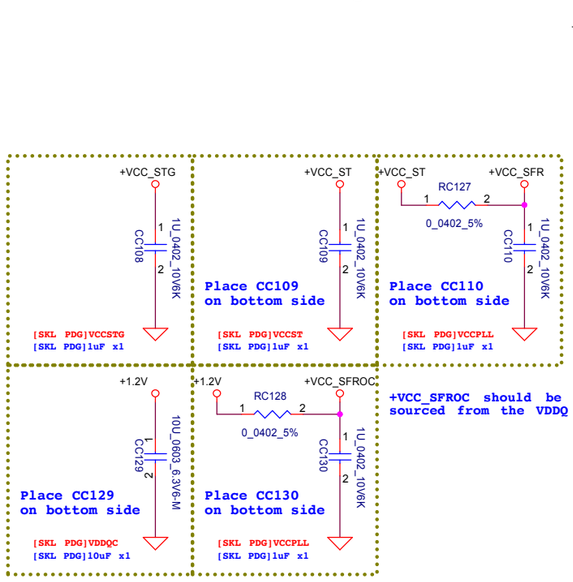
Date: Thursday, August 25, 2016 | Sheet 15 of 82

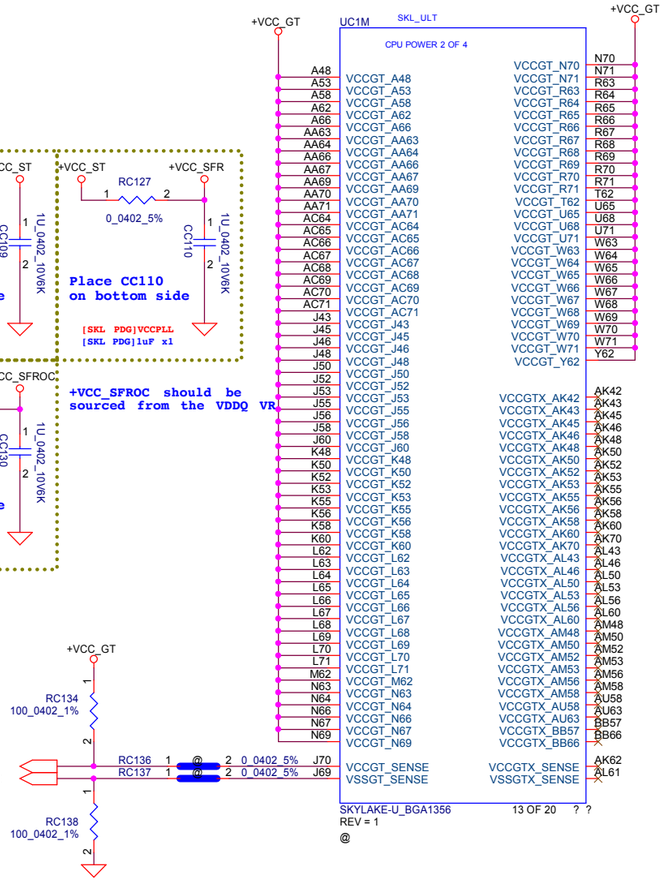
Table 10-10. SVID Bus Routing Guidelines

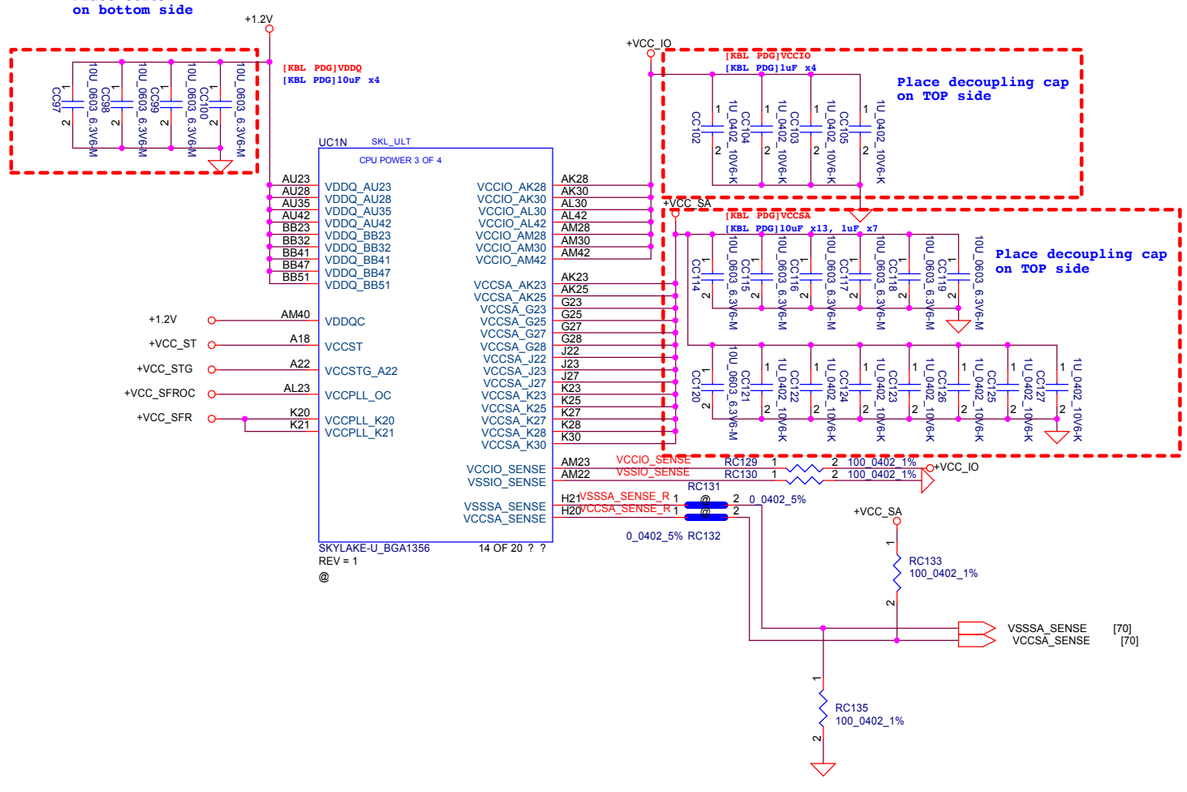
Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	











Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KBL(12/16):POWER**

Size: Custom | Document Number: **SKYWALKER** | Rev: 2.0

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Reserve for Sense Resistor

+1.8VALW — RC139 1 — 2 0_0603_5% — +1.8VALW_PCH
+3VALW — RC140 1 — 2 0_0805_5% — +3VALW_PCH
+1VALW — RC141 1 — 2 0_0805_5% — +1VALW_PCH
+1VALW — RC202 1 — 2 0_0805_5% — +VCC_MPHYGT

+VCC_MPHYGT — RC1451 2 0_0402_5% — +VCC_AMPHYPLL
+1VALW_PCH — RC1461 2 0_0402_5% — +1VALW_PLL

CC132 please close to N18

+VCC_MPHYGT — CC132 1U_0402_10V6K

[SKL PDG]VccAPLLEBB
[SKL PDG]luF x1
[SKL PDG]Close N18,
Placement type:Edge<3mm(118mil)

VccMPHYGT(Mod PHY Externally Gated Primary 1.0 V: Externally gated primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic.)

CC133 & CC134 please close to N15

+VCC_MPHYGT — CC133 1U_0402_10V6K; CC134 47U_0805_6.3V6-M

[SKL PDG]VccMPHYGT
[SKL PDG]luF x1
[SKL PDG]Close N15,
Placement type:Edge<3mm(118mil)
[SKL PDG]47uF x1
[SKL PDG]Close N15,
Placement type:Edge<10mm(394mil)

SRAM Primary Well 1.0 V. Dedicated SRAM rail and can have on board power down gate control.

CC136 please close to AF20

+VCC_MPHYGT — @CC136 1U_0402_10V6K

[SKL PDG]VccSRAM
[SKL PDG]luF x1
[SKL PDG]Close AF20,
Placement type:Edge<10mm(394mil)

Mod PHY Always On Primary 1.0 V: Always on primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic

CC137 please close to K17

+1VALW_PCH — CC137 1U_0402_10V6K

[SKL PDG]VccMPHYAON
[SKL PDG]luF x1
[SKL PDG]Close K17,
Placement type:Edge<3mm(118mil)

please close to AG15 , Y16 & T16

+3VALW_PCH — CC140 1U_0402_10V6K; CC141 1U_0402_10V6K; CC142 1U_0402_10V6K

Primary Well 1.0 V: For I/O blocks, ungated ISH SRAM power, USB AFE Digital Logic, JTAG, Thermal Sensor and MIPI DPHY.

CC143 please close to AB19

+1VALW_PCH — CC143 1U_0402_10V6K

[SKL PDG]VCCPRIM
[SKL PDG]luF x1
[SKL PDG]Close AB19,
Placement type:Edge<10mm(394mil)

+1VALW_PCH — CC181 22U_0603_6.3V6-M; CC131 22U_0603_6.3V6-M
+VCC_MPHYGT — CC182 22U_0603_6.3V6-M; CC135 22U_0603_6.3V6-M

UC1O — SKL_ULT — CPU POWER 4 OF 4

AB19, AB20, P18	VCCPRIM_1P0_AB19, VCCPRIM_1P0_AB20, VCCPRIM_1P0_P18	1100mA
AF18, AF19, V20, V21	VCCPRIM_CORE_AF18, VCCPRIM_CORE_AF19, VCCPRIM_CORE_V20, VCCPRIM_CORE_V21	500mA
+DCPDSW — AL1	DCPDSW_1P0	22mA
K17, L1	VCCMPHYAON_1P0_K17, VCCMPHYAON_1P0_L1	
N15, N16, N17, P15, P16	VCCMPHYGT_1P0_N15, VCCMPHYGT_1P0_N16, VCCMPHYGT_1P0_N17, VCCMPHYGT_1P0_P15, VCCMPHYGT_1P0_P16	1500mA
+VCC_AMPHYPLL — K15, L15	VCCAMPHYPLL_1P0_K15, VCCAMPHYPLL_1P0_L15	88mA
+1VALW_PLL — V15	VCAPLL_1P0	26mA
AB17, Y18	VCCPRIM_1P0_AB17, VCCPRIM_1P0_Y18	
+VCC_DSW3P3 — AD17, AD18, AJ17	VCCDSW_3P3_AD17, VCCDSW_3P3_AD18, VCCDSW_3P3_AJ17	118mA
+VCC_HDA — AJ19	VCCHDA	68mA
+3V_SPI — AJ16	VCCSPI	
AF20, AF21, T19, T20	VCCSRAM_1P0_AF20, VCCSRAM_1P0_AF21, VCCSRAM_1P0_T19, VCCSRAM_1P0_T20	565mA
+3VALW_PRIM — AJ21	VCCPRIM_3P3_AJ21	75mA
AK20	VCCPRIM_1P0_AK20	33mA
N18	VCCAPLLEBB	33mA

SKYLAKE-U_BGA1356
REV = 1
@
15 OF 20 ? ?

VCCPGPPA, VCCPGPPB, VCCPGPPC, VCCPGPPD, VCCPGPPE, VCCPGPPF, VCCPGPPG	AK15, AG15, Y16, Y15, T16, AF16, AD15	85mA +3VALW_PCH
VCCPRIM_3P3_V19	V19	161mA +1.8VALW_PCH; +3VALW_PRIM
VCCPRIM_1P0_T1	T1	135mA +1VALW_PCH; +1.8VALW_PCH
VCCATS_1P8	AA1	+3VALW_RTCPRIM
VCCRTCPRIM_3P3	AK17	+RTCVCC
VCCRTC_AK19, VCCRTC_BB14	AK19, BB14	
DCPRTC — +DCPRTC	BB10	
VCCCLK1	A14	
VCCCLK2	K19	
VCCCLK3	L21	
VCCCLK4	N20	
VCCCLK5	L19	
VCCCLK6	A10	
GPP_B0/CORE_VID0, GPP_B1/CORE_VID1	AN11, AN13	T1, T2

Primary Well 3.3 V

+3VALW_PCH — RC147 1 — 2 0_0402_5% — +3VALW_PRIM; +3VALW_PRIM — CC145 1U_0402_10V6K

[SKL PDG]VCCPRIM
[SKL PDG]luF x1
[SKL PDG]Close V19,
Placement type:Edge<3mm(118mil)

HD Audio Power 3.3 V, 1.8 V, 1.5 V. For Intel High Definition Audio.

+3VALW_PCH — RC148 1 — 2 0_0402_5% — +VCC_HDA; +VCC_HDA — CC147 1U_0402_10V6K

[SKL PDG]VccHDA
[SKL PDG]luF x1
[SKL PDG]Close AJ19,
Placement type:Edge<10mm(394mil)

Thermal Sensor Primary Well 1.8 V

+1.8VALW_PCH — CC144 1U_0402_10V6K

[SKL PDG]VccATS
[SKL PDG]luF x1
[SKL PDG]Close AA1,
Placement type:Edge<10mm(394mil)

Deep Sx Well 1.0 V: This rail is generated by on die DSW low dropout (LDO) linear voltage regulator to supply DSW GPIOs, DSW core logic and DSW USB2 logic. Board needs to connect 1 uF capacitor to this rail and power should NOT be driven from the board. When primary well power is up, this rail is bypassed from VCCPRIM_1p0.

+DCPDSW — CC148 1U_0402_10V6K

[SKL PDG]DcpDSW
[SKL PDG]luF x1
[SKL PDG]Close AL1,
Placement type:Edge<3mm(118mil)

RTC de-coupling capacitor only. This rail should NOT be driven.

+DCPRTC — CC146 0.1U_0402_10V6-K

[SKL PDG]DcpRTC
[SKL PDG]0.1uF x1
[SKL PDG]Close BB10,
Placement type:Edge<3mm(118mil)

+VCC_AMPHYPLL — @CC149 1U_0402_10V6K

Core Logic Primary Well: This rail scales from 0.85 V to 1.0 V.

+1VALW — RC151 1 — 2 0_0805_5% — +PCH_CORE; +PCH_CORE — CC150 1U_0402_10V6K

[SKL PDG]VccPRIM_Core
[SKL PDG]luF x1
[SKL PDG]Close AF18,
Placement type:Edge<10mm(394mil)

Deep Sx Well for GPD GPIOs and USB2

+3VALW_PCH — RC152 1 — 2 0_0402_5% — +VCC_DSW3P3

[SKL PDG]VccDSW

RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.

+3VALW_PCH — RC150 1 — 2 0_0402_5% — +3VALW_RTCPRIM
+3VALW_RTCPRIM — CC151 1U_0402_10V6K; CC152 0.1U_0402_10V6K; CC153 0.1U_0402_10V6K

[SKL PDG]VccRTCPRIM
[SKL PDG]luF x1,0.1uF x2
[SKL PDG]Close AK17,
Placement type:Edge<3mm(118mil)

RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.

+RTCVCC — CC154 1U_0402_10V6K

[SKL PDG]VccRTC
[SKL PDG]luF x1
[SKL PDG]Close AK19,
Placement type:Edge<3mm(118mil)

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Title: **KBL(13/16):POWER**

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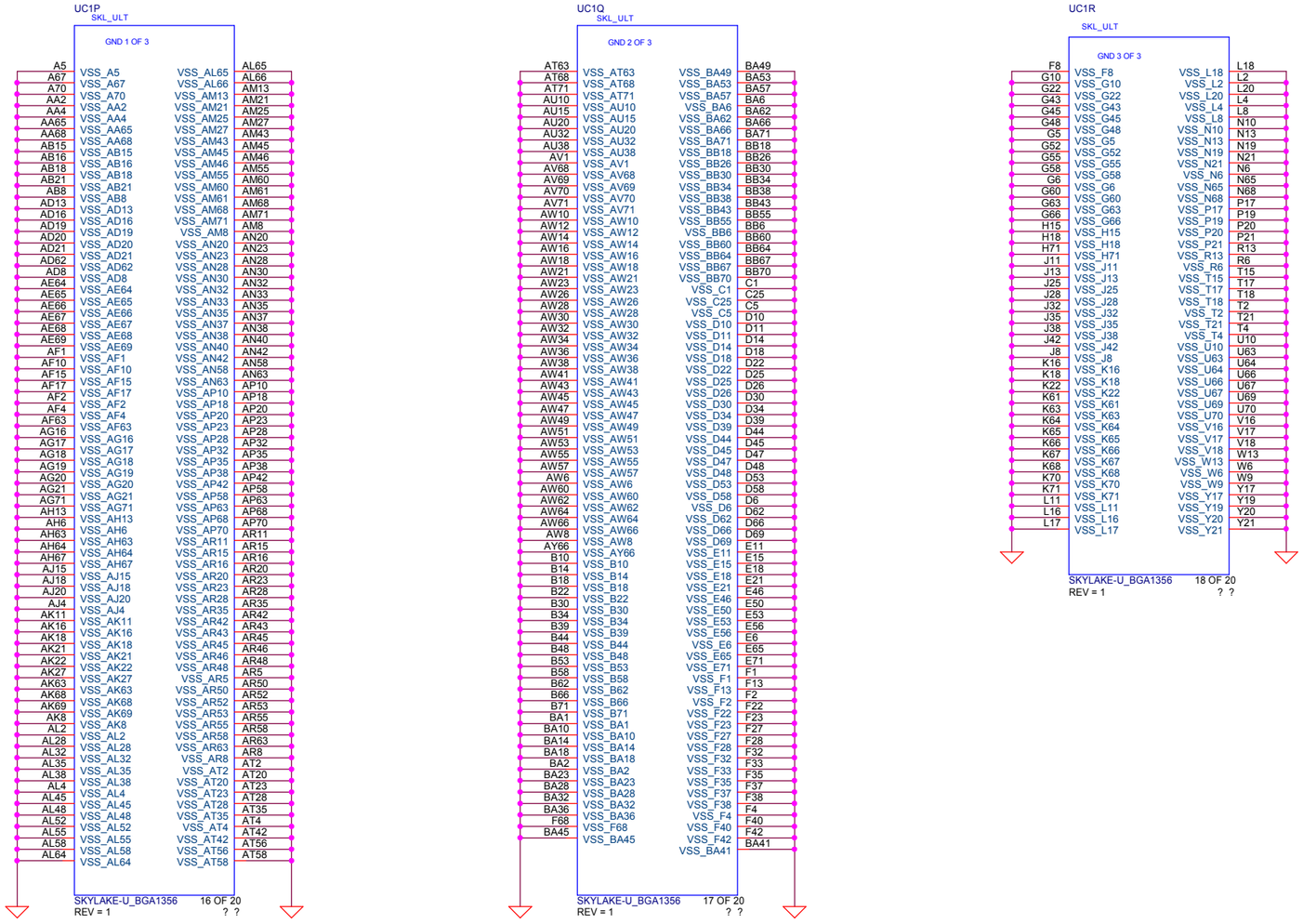

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Title: **KBL(14/16):GND**

Size	Document Number	Rev
Custom	SKYWALKER	2.0

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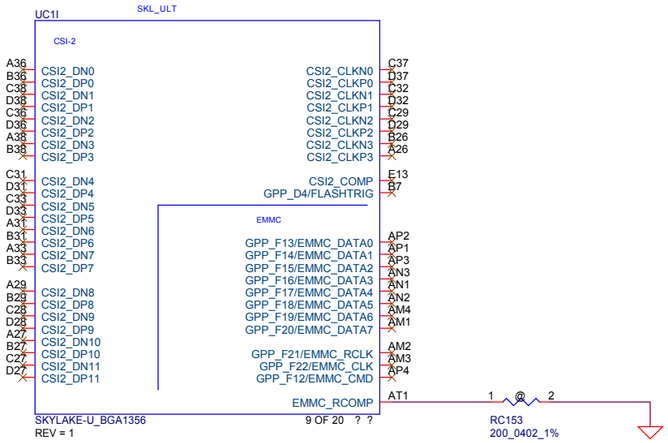

Security Classification	LC Future Center Secret Data		
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Title: **KBL(15/16):CSI-2/EMMC**

Size	Document Number	Rev
Custom	SKYWALKER	2.0

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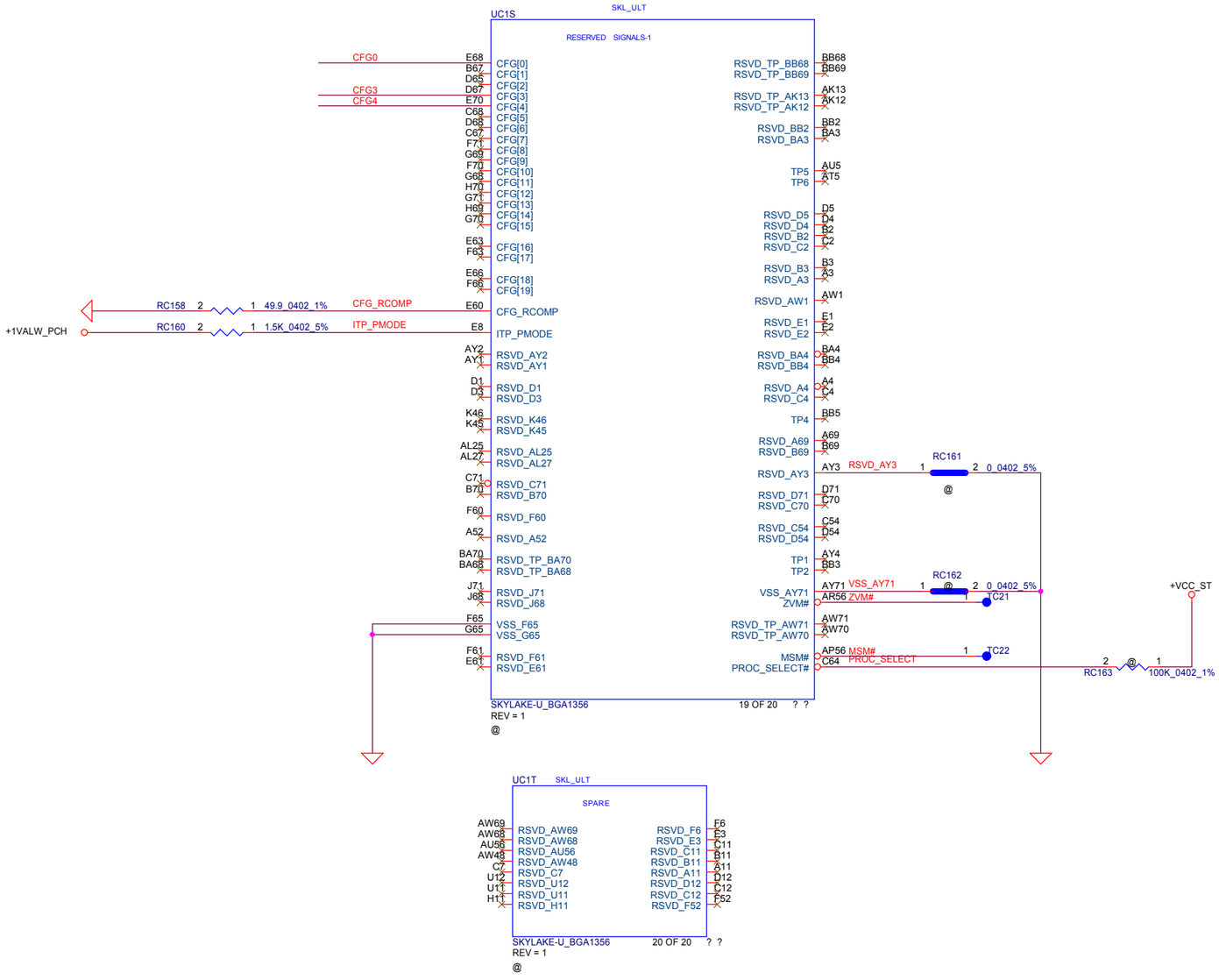

[SKL EDS]

CFG0

+VCC_IO

CFG0 — RC154 2 @ 1 1K_0402_5%

RC155 2 @ 1 1K_0402_1%

L:Stall.
*H:(Default) Normal Operation; No stall.

CFG4

+VCC_IO

CFG4 — RC156 2 @ 1 1K_0402_5%

RC157 2 1 1K_0402_1%

*L: Embedded DisplayPort Enabled
H: Embedded DisplayPort Disabled

CFG3

CFG3 — RC159 1 @ 2 1K_0402_5%

CFG3 require >= 0.5"
CPU Debug Consent Strap

TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted
1 : No Stall
0 : Stall

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

Security Classification	LC Future Center Secret Data		
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Title: KBL(16/16):CFG/RESERVED

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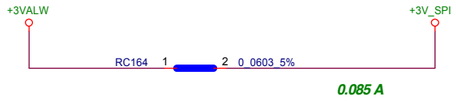
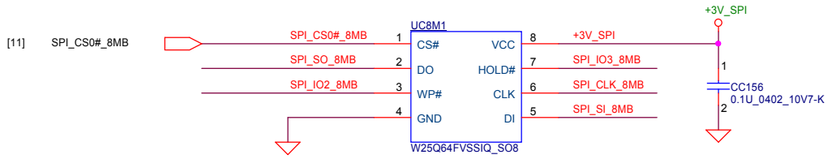
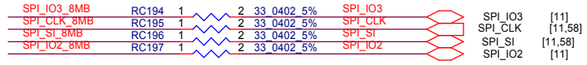


8MB(64Mb)

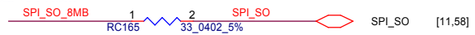
[SKL]SPI0_CS0#: SPI FLASH
SPI0_CS1#: SPI FLASH
SPI0_CS2#: SPI TPM



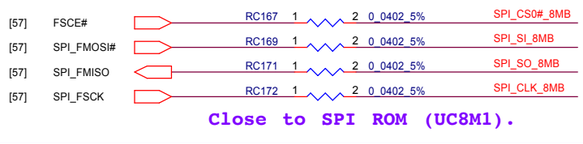
Place RC194,195,196,197 close together



Near SPI ROM

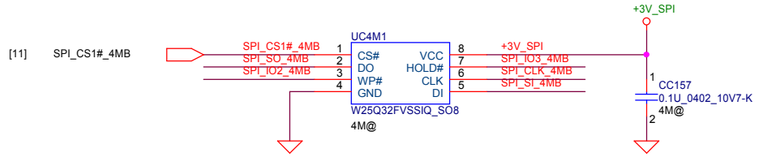


Mirror Code



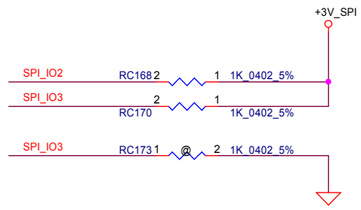
Close to SPI ROM (UC8M1).

4MB(32Mb) Reserve



Place RC203,204,205,206 close together

Near SPI ROM



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Title: SPI ROM

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Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins.
330uF placeholder

[KBL PDG]VDDQ
[KBL PDG] EE 10uF x16, 1uF x16. 330uF x1

+1.2V

CD1 10U_0603_6.3V6-M
CD2 10U_0603_6.3V6-M
CD3 10U_0603_6.3V6-M
CD4 10U_0603_6.3V6-M
CD5 10U_0603_6.3V6-M
CD6 10U_0603_6.3V6-M
CD7 10U_0603_6.3V6-M
CD8 10U_0603_6.3V6-M

+1.2V

CD14 1U_0402_6.3V6-K
CD15 1U_0402_6.3V6-K
CD16 1U_0402_6.3V6-K
CD17 1U_0402_6.3V6-K
CD18 1U_0402_6.3V6-K
CD19 1U_0402_6.3V6-K
CD20 1U_0402_6.3V6-K
CD21 1U_0402_6.3V6-K
CD26 330U_D2_2VM_R9M @

Place decoupling cap on DRAM side.

[KBL PDG]VPP
[KBL PDG] EE 10uF x2, 1uF x2.

+2.5V

CD9 10U_0603_6.3V6-M
CD10 10U_0603_6.3V6-M
CD11 1U_0402_6.3V6-K
CD12 1U_0402_6.3V6-K

Place decoupling on the VTT plane close to SODIMM

[KBL PDG]VTT
[KBL PDG] EE 10uF x2, 1uF x4.

+0.6VS

CD22 10U_0603_6.3V6-M
CD23 10U_0603_6.3V6-M
CD24 1U_0402_6.3V6-K
CD63 1U_0402_6.3V6-K
CD64 1U_0402_6.3V6-K
CD65 1U_0402_6.3V6-K

DDR_A_D[0..63] [7]
DDR_A_MA[0..16] [7]
DDR_A_DQS#[0..7] [7]
DDR_A_DQS[0..7] [7]

JDIMM1A ME@

+1.2V

DDR_A_D5	1	VSS_1	VSS_2	2	
	3	DQ5	DQ4	4	DDR_A_D0
DDR_A_D1	5	VSS_3	VSS_4	6	DDR_A_D4
	7	DQ1	DQ0	8	
DDR_A_DQS#0	9	VSS_5	VSS_6	10	
DDR_A_DQS0	11	DQS0_C	DM0_n/DBI0_n	12	
	13	DQS0_t	VSS_7	14	
DDR_A_D2	15	VSS_8	DQ6	16	DDR_A_D6
	17	DQ7	VSS_9	18	
DDR_A_D7	19	VSS_10	DQ2	20	DDR_A_D3
	21	DQ3	VSS_11	22	
DDR_A_D9	23	VSS_12	DQ12	24	DDR_A_D8
	25	DQ13	VSS_13	26	
DDR_A_D12	27	VSS_14	DQ8	28	DDR_A_D13
	29	DQ9	VSS_15	30	
	31	VSS_16	DQS1_c	32	DDR_A_DQS#1
	33	DM1_n/DBI1_n	DQS1_t	34	DDR_A_DQS1
DDR_A_D10	35	VSS_17	VSS_18	36	
	37	DQ15	DQ14	38	DDR_A_D11
DDR_A_D15	39	VSS_19	VSS_20	40	
	41	DQ10	DQ11	42	DDR_A_D14
DDR_A_D16	43	VSS_21	VSS_22	44	
	45	DQ21	DQ20	46	DDR_A_D17
DDR_A_D20	47	VSS_23	VSS_24	48	
	49	DQ17	DQ16	50	DDR_A_D21
DDR_A_DQS#2	51	VSS_25	VSS_26	52	
DDR_A_DQS2	53	DQS2_c	DM2_n/DBI2_n	54	
	55	DQS2_t	VSS_27	56	
DDR_A_D23	57	VSS_28	DQ22	58	DDR_A_D22
	59	DQ23	VSS_29	60	
DDR_A_D18	61	VSS_30	DQ18	62	DDR_A_D19
	63	DQ19	VSS_31	64	
DDR_A_D25	65	VSS_32	DQ28	66	DDR_A_D29
	67	DQ29	VSS_33	68	
DDR_A_D24	69	VSS_34	DQ24	70	DDR_A_D28
	71	DQ25	VSS_35	72	
	73	VSS_36	DQS3_c	74	DDR_A_DQS#3
	75	DM3_n/DBI3_n	DQS3_t	76	DDR_A_DQS3
DDR_A_D30	77	VSS_37	VSS_38	78	
	79	DQ30	DQ31	80	DDR_A_D31
DDR_A_D26	81	VSS_39	DQ28	82	DDR_A_D27
	83	DQ28	DQ27	84	
	85	VSS_41	VSS_42	86	
	87	CB5/NC	CB4/NC	88	
	89	VSS_43	VSS_44	90	
	91	CB1/NC	CB0/NC	92	
	93	VSS_45	VSS_46	94	
DDR_A_DQS#8	95	DQS8_c	DM8_n/DBI8_n/NC	96	
DDR_A_DQS8	97	DQS8_t	VSS_47	98	
	99	VSS_48	CB6/NC	100	
	101	CB2/NC	VSS_49	102	
	103	VSS_50	CB7/NC	104	
	105	CB3/NC	VSS_51	106	
	107	VSS_52	RESET_n	108	DDR4_DRAMRST# [8,23]
DDR_A_CKE0	109	CKE0	CKE1	110	DDR_A_CKE1 [7]
DDR_A_BG1	111	VDD_1	VDD_2	112	
DDR_A_BG0	113	BG1	ACT_n	114	DDR_A_ACT_N
	115	BG0	ALERT_n	116	DDR_A_ALERT_N
DDR_A_MA12	117	VDD_3	VDD_4	118	
DDR_A_MA9	119	A12	A11	120	DDR_A_MA11
	121	A9	A7	122	DDR_A_MA7
DDR_A_MA8	123	VDD_5	VDD_6	124	
DDR_A_MA6	125	A8	A5	126	DDR_A_MA5
	127	A6	A4	128	DDR_A_MA4
	129	VDD_7	VDD_8	130	

FOX_AS0A826-H4RB-7H

[7] DDR_A_CKE0
[7] DDR_A_BG1
[7] DDR_A_BG0

+3VS

RD6 10K_0402_5% @ — SA0_CHA_P — RD9 0_0402_5%
RD7 10K_0402_5% @ — SA1_CHA_P — RD10 0_0402_5%
RD8 10K_0402_5% @ — SA2_CHA_P — RD11 0_0402_5%

SPD Address = 0H

JDIMM1B ME@

+2.5V +1.2V +0.6VS

DDR_A_MA3	131	A3	A2	132	DDR_A_MA2
DDR_A_MA1	133	A1	EVENT_n/NF	134	EVENT_n_t
	135	VDD_9	VDD_10	136	
[7] DDR_A_DDRCLK0_1866M	137	CK0_t	CK1_t/NF	138	DDR_A_DDRCLK1_1866M
[7] DDR_A_DDRCLK0_1866M#	139	CK0_c	CK1_c/NF	140	DDR_A_DDRCLK1_1866M#
DDR_A_PARITY	141	VDD_11	VDD_12	142	
[7] DDR_A_PARITY	143	Parity	A0	144	DDR_A_MA0
DDR_A_BA1	145	BA1	A10/AP	146	DDR_A_MA10
[7] DDR_A_BA1	147	VDD_13	VDD_14	148	
DDR_A_CS0#	149	CS0_n	BA0	150	DDR_A_BA0
[7] DDR_A_CS0#	151	A14/WE_n	A16/RAS_n	152	DDR_A_MA16
DDR_A_MA14	153	VDD_15	VDD_16	154	
DDR_A_ODT0	155	ODT0	A15/CAS_n	156	DDR_A_MA15
DDR_A_CS1#	157	CS1_n	A13	158	DDR_A_MA13
[7] DDR_A_ODT0	159	VDD_17	VDD_18	160	
[7] DDR_A_CS1#	161	ODT1	C0/CS2_n/NC	162	
DDR_A_ODT1	163	VDD_19	VREFCA	164	M_VREF_CA_DIMMA
[7] DDR_A_ODT1	165	C1/CS3_n/NC	SA2	166	SA2_CHA_P
	167	VSS_53	VSS_54	168	
DDR_A_D37	169	DQ37	DQ36	170	DDR_A_D33
	171	VSS_55	VSS_56	172	
DDR_A_D32	173	DQ33	DQ32	174	DDR_A_D36
	175	VSS_57	VSS_58	176	
DDR_A_DQS#4	177	DQS4_c	DM4_n/DBI4_n	178	
DDR_A_DQS4	179	DQS4_t	VSS_59	180	
	181	VSS_60	DQ39	182	DDR_A_D35
DDR_A_D38	183	DQ38	DQ35	184	
	185	VSS_61	VSS_62	186	DDR_A_D34
DDR_A_D39	187	VSS_62	DQ34	188	
	189	DQ34	VSS_63	190	DDR_A_D41
DDR_A_D40	191	VSS_64	DQ45	192	
	193	DQ44	VSS_65	194	DDR_A_D45
DDR_A_D44	195	VSS_66	DQ41	196	
	197	DQ40	VSS_67	198	DDR_A_DQS#5
	199	VSS_68	DQS5_c	200	DDR_A_DQS5
	201	DM5_n/DBI5_n	DQS5_t	202	
DDR_A_D43	203	VSS_69	VSS_70	204	DDR_A_D42
	205	DQ46	DQ47	206	
DDR_A_D46	207	VSS_71	VSS_72	208	DDR_A_D47
	209	DQ42	DQ43	210	
DDR_A_D49	211	VSS_73	VSS_74	212	DDR_A_D48
	213	DQ52	DQ53	214	
DDR_A_D52	215	VSS_75	VSS_76	216	DDR_A_D53
	217	DQ49	DQ48	218	
DDR_A_DQS#6	219	VSS_77	VSS_78	220	
DDR_A_DQS6	221	DQS6_c	DM6_n/DBI6_n	222	
DDR_A_D50	223	DQS6_t	VSS_79	224	DDR_A_D54
	225	VSS_80	DQ54	226	
DDR_A_D55	227	DQS5	VSS_81	228	DDR_A_D51
	229	VSS_82	DQ50	230	
DDR_A_D56	231	DQ51	VSS_83	232	DDR_A_D57
	233	VSS_84	DQ60	234	
DDR_A_D60	235	DQ61	VSS_85	236	DDR_A_D61
	237	VSS_86	DQ57	238	
	239	DQ56	VSS_87	240	DDR_A_DQS#7
	241	VSS_88	DQS7_c	242	DDR_A_DQS7
DDR_A_D59	243	DM7_n/DBI7_n	DQS7_t	244	
	245	VSS_89	VSS_90	246	DDR_A_D63
DDR_A_D58	247	DQ62	DQ63	248	
	249	VSS_91	VSS_92	250	DDR_A_D62
CP_SMB_CLK	251	DQ58	DQ59	252	
	253	VSS_93	VSS_94	254	CP_SMB_DAT
	255	SCL	SDA	256	SA0_CHA_P
	257	VDDSPD	SA0	258	
	259	VPP_1	VTT	260	SA1_CHA_P
	261	VPP_2	SA1	262	
		GND_1	GND_2		

FOX_AS0A826-H4RB-7H

RF

RD5 240_0402_1%

DDR_A_BA0 [7]
CP_SMB_DAT [11,23,63]

CD27 2.2U_0402_6.3V6-M @
CD28 0.1U_0402_10V7-K @

+3VS

RD12 0_0402_5% @
[11,23,63] CP_SMB_CLK

[KBL PDG]VDDSPD
[KBL PDG] EE 0.1uF x1, 2.2uF x1.

CD29 0.1U_0402_10V7-K
CD30 2.2U_0402_6.3V6-M

Place decoupling cap close to DIMM

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-R5	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

+1.2V

RD1 1K_0402_1%
RD2 2_0402_1%
RD3 1K_0402_1%
RD4 24.9_0402_1%
CD13 0.022U_0402_25V7-K
CD25 0.1U_0402_16V7-K @

[7] DDR4_VREF_CA_CPU_A
M_VREF_CA_DIMMA

+1.2V

RD13 240_0402_1%
RD14 240_0402_1%

DDR_A_DQS#8
DDR_A_DQS8

Security Classification	LC Future Center Secret Data			Title	DDR4 CH-A PRIMARY
Issued Date	2015/09/01	Deciphered Date	2016/12/31		
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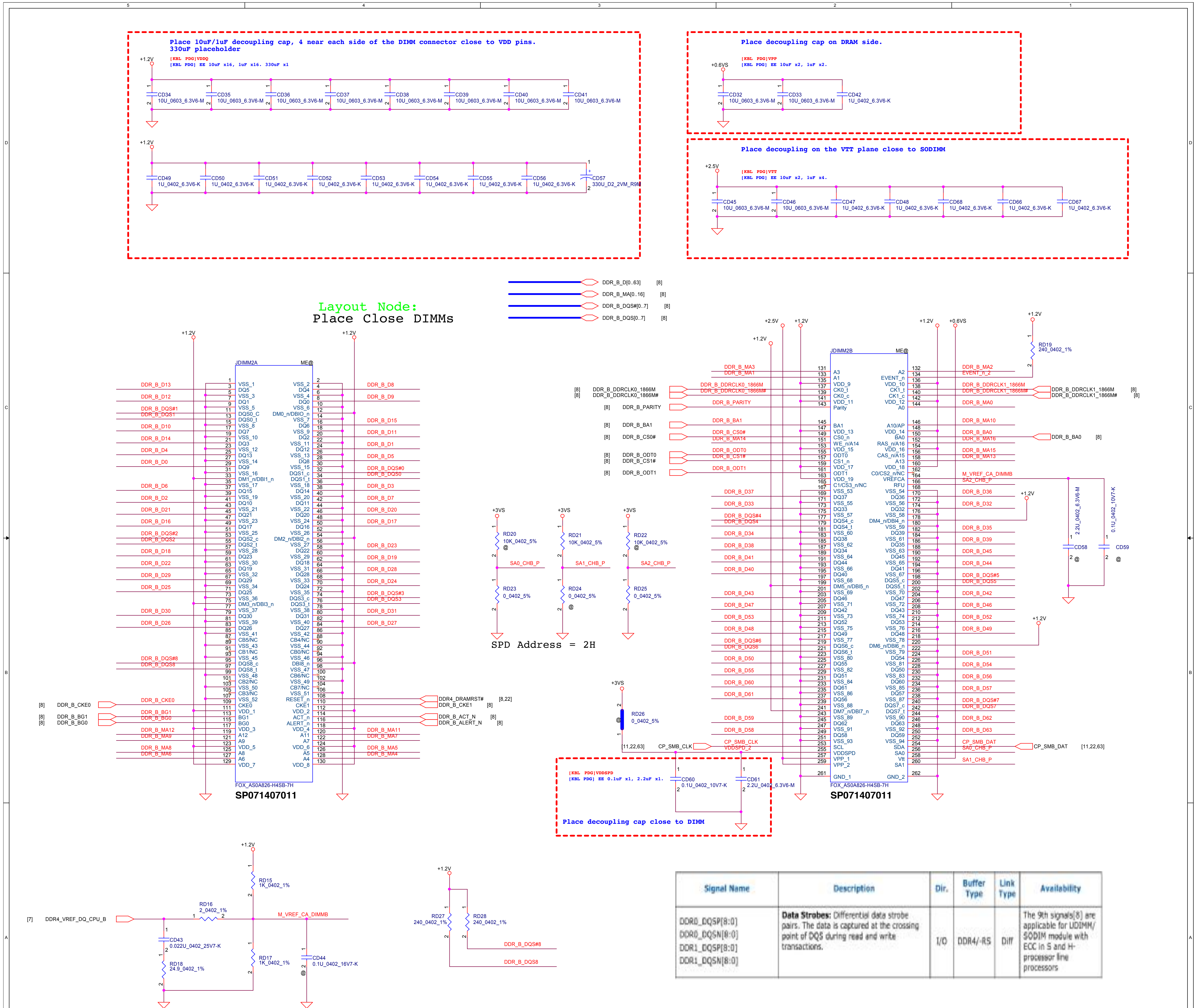

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-RS	Diff	The 9th signals[8] are applicable for UDIMM/ SODIMM module with ECC in S and H-processor line processors.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **DDR4 CH-B PRIMARY**

Size: Custom | Document Number: **SKYWALKER** | Rev: 2.0

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_AON	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VS_AON	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_AON	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_AON	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VS_AON	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VS_AON				
STRAP3	+3VS_AON				
STRAP4	+3VS_AON				

DEVID_SEL	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

PCIE_CFG	
0	(Default)
1	

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

X76

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16P-GT	Samsung	K4G41325FE-HC28	PD 45.3K	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5GC4H24AJR-T2C 256X16	PD 34.8K							
	Micron	EDW4032BABG-60-F 256X16	PD 24.9K							

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR	Samsung	K4G80325FB-HC03	PD 4.99K	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5GC8H24MJR-T2C	PD 30.1K							
	Micron	MT51J256M32HF-60:A	PD 10K							

Title			
VGA NOTE			
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[15] PCIE_CTX_C_GRX_N[1..4]
[15] PCIE_CTX_C_GRX_P[1..4]
PCIE_CTX_C_GRX_N[1..4]
PCIE_CTX_C_GRX_P[1..4]
[15] PCIE_CRX_GTX_N[1..4]
[15] PCIE_CRX_GTX_P[1..4]
PCIE_CRX_GTX_N[1..4]
PCIE_CRX_GTX_P[1..4]

+3VS_AON
RV1 @ 10K_0402_5%
UV1A
1/18 PCI_EXPRESS
GM107/GM108 GK107/GK208 GF117
AJ11 PEX_WAKE_N — NC
[28] VGA_PEX_RST# — VGA_PEX_RST# — RV11 DIS@ 0_0402_5%
AJ12 PEX_RST_N
CLKREQ_VGA# — AK12 PEX_CLKREQ_N
[10] CLK_PCIE_VGA — CLK_PCIE_VGA — AL13 PEX_REFCLK
[10] CLK_PCIE_VGA# — CLK_PCIE_VGA# — AK13 PEX_REFCLK_N

PCIE_CRX_GTX_P1 — CV8 — PCIE_CRX_C_GTX_P1 — AK14 PEX_TX0
PCIE_CRX_GTX_N1 — CV9 — PCIE_CRX_C_GTX_N1 — AJ14 PEX_TX0_N
PCIE_CTX_C_GRX_P1 — AN12 PEX_RX0
PCIE_CTX_C_GRX_N1 — AM12 PEX_RX0_N
PCIE_CRX_GTX_P2 — CV10 — PCIE_CRX_C_GTX_P2 — AH14 PEX_TX1
PCIE_CRX_GTX_N2 — CV11 — PCIE_CRX_C_GTX_N2 — AG14 PEX_TX1_N
PCIE_CTX_C_GRX_P2 — AN14 PEX_RX1
PCIE_CTX_C_GRX_N2 — AM14 PEX_RX1_N
PCIE_CRX_GTX_P3 — CV12 — PCIE_CRX_C_GTX_P3 — AK15 PEX_TX2
PCIE_CRX_GTX_N3 — CV13 — PCIE_CRX_C_GTX_N3 — AJ15 PEX_TX2_N
PCIE_CTX_C_GRX_P3 — AP14 PEX_RX2
PCIE_CTX_C_GRX_N3 — AP15 PEX_RX2_N
PCIE_CRX_GTX_P4 — CV21 — PCIE_CRX_C_GTX_P4 — AL16 PEX_TX3
PCIE_CRX_GTX_N4 — CV22 — PCIE_CRX_C_GTX_N4 — AK16 PEX_TX3_N
PCIE_CTX_C_GRX_P4 — AN15 PEX_RX3
PCIE_CTX_C_GRX_N4 — AM15 PEX_RX3_N

AK17 PEX_TX4
AJ17 PEX_TX4_N
AN17 PEX_RX4
AM17 PEX_RX4_N
AH17 PEX_TX5
AG17 PEX_TX5_N
AP17 PEX_RX5
AP18 PEX_RX5_N
AK18 PEX_TX6
AJ18 PEX_TX6_N
AN18 PEX_RX6
AM18 PEX_RX6_N
AL19 PEX_TX7
AK19 PEX_TX7_N
AN20 PEX_RX7
AM20 PEX_RX7_N
AK20 PEX_TX8
AJ20 PEX_TX8_N
AP20 PEX_RX8
AP21 PEX_RX8_N
AH20 PEX_TX9
AG20 PEX_TX9_N
AN21 PEX_RX9
AM21 PEX_RX9_N
AK21 PEX_TX10
AJ21 PEX_TX10_N
AN23 PEX_RX10
AM23 PEX_RX10_N
AL22 PEX_TX11
AK22 PEX_TX11_N
AP23 PEX_RX11
AP24 PEX_RX11_N
AK23 PEX_TX12
AJ23 PEX_TX12_N
AN24 PEX_RX12
AM24 PEX_RX12_N
AH23 PEX_TX13
AG23 PEX_TX13_N
AN26 PEX_RX13
AM26 PEX_RX13_N
AK24 PEX_TX14
AJ24 PEX_TX14_N
AP26 PEX_RX14
AP27 PEX_RX14_N
AL25 PEX_TX15
AK25 PEX_TX15_N
AN27 PEX_RX15
AM27 PEX_RX15_N
PEX LANES 4 TO 15 NC FOR GM108
PEX LANES 8 TO 15 NC FOR GK208/GF117
N16P-GX_BGA908

PEX_IOVDD_1 AG19
PEX_IOVDD_2 AG21
PEX_IOVDD_3 AG22
PEX_IOVDD_4 AG24
PEX_IOVDD_5 AH21
PEX_IOVDD_6 AH25
PEX_IOVDDQ_01 AG13
PEX_IOVDDQ_02 AG15
PEX_IOVDDQ_03 AG16
PEX_IOVDDQ_04 AG18
PEX_IOVDDQ_05 AG25
PEX_IOVDDQ_06 AH15
PEX_IOVDDQ_07 AH18
PEX_IOVDDQ_08 AH26
PEX_IOVDDQ_09 AH27
PEX_IOVDDQ_10 AJ27
PEX_IOVDDQ_11 AK27
PEX_IOVDDQ_12 AL27
PEX_IOVDDQ_13 AM28
PEX_IOVDDQ_14 AN28

+1.05VS_VGA
Under GPU
Near GPU
Midway between GPU and power supply
1UF_0402_6.3V6-K CV54 DIS@
1UF_0402_6.3V6-K CV55 DIS@
4.7U_0603_6.3VAK CV3 DIS@
10U_0603_6.3V6M CV4 DIS@
10U_0603_6.3V6M CV67 DIS@
22U_0603_6.3V6-M CV64 DIS@
22U_0603_6.3V6-M CV7 DIS@
1UF_0402_6.3V6-K CV56 DIS@
1UF_0402_6.3V6-K CV57 DIS@
4.7U_0603_6.3VAK CV16 DIS@
10U_0603_6.3V6M CV17 DIS@
10U_0603_6.3V6M CV61 DIS@
22U_0603_6.3V6-M CV58 DIS@
22U_0603_6.3V6-M CV20 DIS@

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
+3VS_AON
0.1U_0402_10V7-K CV23 DIS@
4.7U_0402_6.3V6M CV24 DIS@
4.7U_0402_6.3V6M CV25 DIS@

+VGA_CORE
100_0402_1% RV2 DIS@
VDD_SENSE L4 — GFXCORE_VDD_SENSE_D [75]
GND_SENSE L5 — GFXCORE_GND_SENSE_D [75]
100_0402_1% RV3 DIS@

3V3AUX_NC P8

PEX_TSTCLK_OUT AJ26
PEX_TSTCLK_OUT_N AK26
RV6 @ 200_0402_1%
+1.05VS_VGA
0_0402_5% RV7 DIS@
PEX_PLLVDD AG26
Under GPU: CV26 DIS@ 0.1U_0402_25V7K
Near GPU: CV27 DIS@ 1UF_0402_6.3V6-K; CV28 DIS@ 4.7U_0402_6.3V6M
TESTMODE AK11
PEX_TERMP AP29
RV10 DIS@ 2.49K_0402_1%
RV8 DIS@ 10K_0402_5%

+3VS_AON
RV13 10K_0402_5% DIS@
[80] dgpu_pwrgd — dgpu_pwrgd
[79] VDDQPWRGD — VDDQPWRGD
DV1
All_GPU_PWRGD — All_GPU_PWRGD [11]
BAT54AW_SOT323-3 DIS@
+3VS
RV9212 DIS@ 10K_0402_5% dgpu_pwrgd
RV9222 DIS@ 10K_0402_5% VDDQPWRGD

+3VS_AON
+3VS_AON
RV5 10K_0402_5% DIS@
[10] CLKREQ_PCIE4_VGA# — DIS@ — CLKREQ_VGA#
QV1 2N7002KW_SOT323-3
RV9 10K_0402_5% @
RV14 @ 0_0402_5%

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: N16P-Q1/Q3(1/6): PEG I/F
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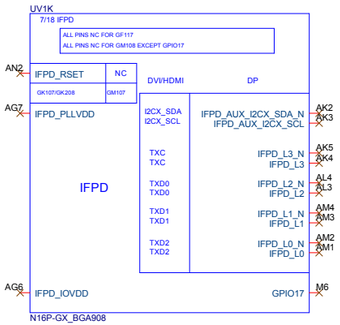

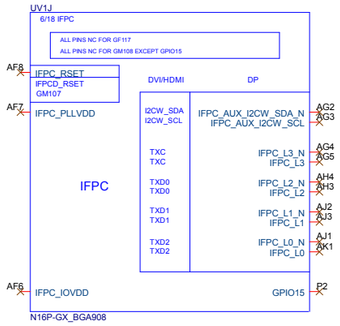

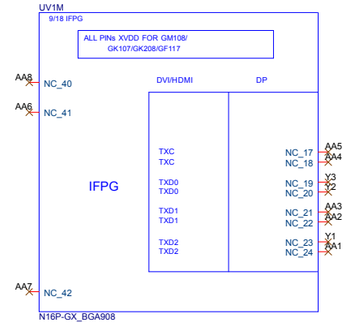

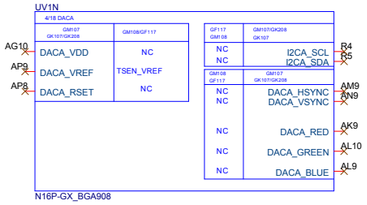

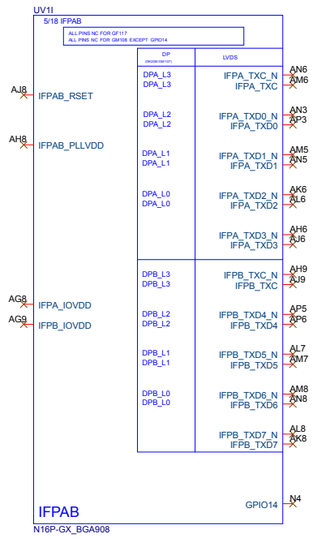

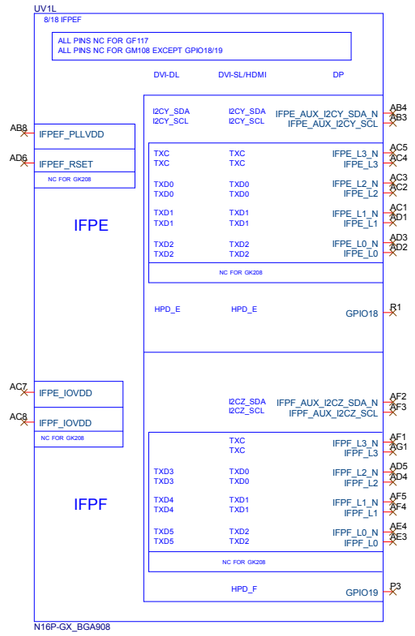

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **N16P-Q1/Q3(2/6): DIGITAL OUT**

Size	Document Number	Rev
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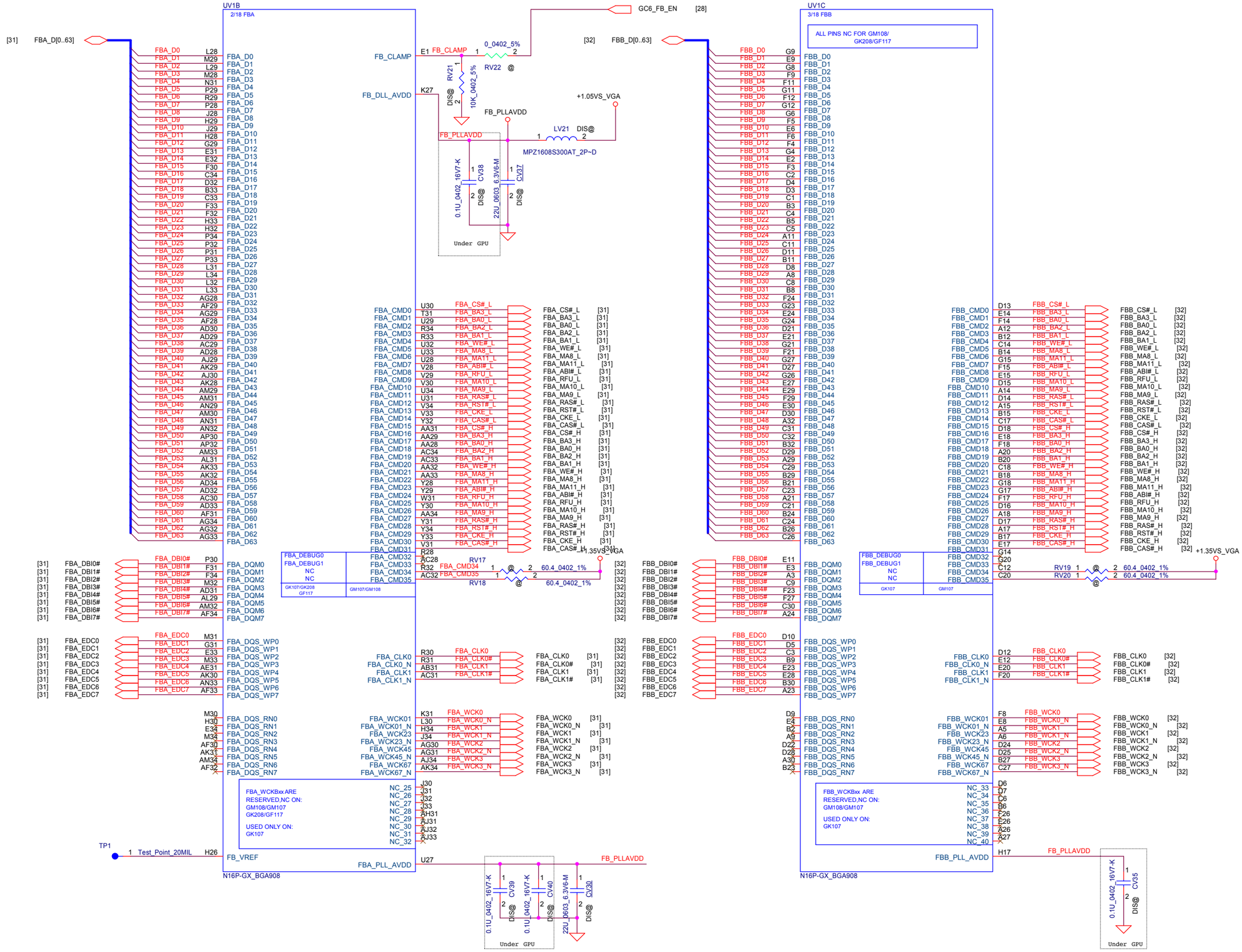

FBx_PLL_AVDD		
Capactior Type	GB4B-128/GDDR5 NV_DG	Actual
0.1uF_0402	3	3
22uF_0805	1	1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: 033_N16P-Q1/Q3(3/6): MEM

Size	Document Number	Rev
Custom	SKYWALKER	2.0

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52mA

30ohm@100MHz ESR=0.01

+1.05VS_VGA

LV1 DIS@ MPZ1608S300AT_2P~D NEAR BALL

CV107 DIS@ 22U_0603_6.3V6-M

CV108 DIS@ 0.1U_0402_25V7K

112mA

LV2 PBY160808T-301Y-N_2P DIS@

CV101 DIS@ 22U_0603_6.3V6-M

CV102 DIS@ 10U_0603_6.3V6-M

CV103 DIS@ 0.1U_0402_25V7K

CV104 DIS@ 0.1U_0402_25V7K

UNDER GPU

RV104 DIS@ 0_0402_5%

VIDEO_CLK_XTAL_SS

50-ohm TRACE

UV1P 12/18 XTAL_PLL

AD8 PLLVDD
AE8 SP_PLLVDD
AD7 VID_PLLVDD | NC
GM107 GK107/GK208 | GM108 GF117

H1 XTAL_SSIN
H3 XTAL_IN
J4 XTAL_OUTBUFF
H2 XTAL_OUT

N16P-GX_BGA908

+3VS_AON

RV125 @ 10K_0402_5%

RV109 DIS@ 10K_0402_5%

XTAL_OUTBUFF_GPU

RV108 DIS@ 10K_0402_5%

RV110 @ 1M_0402_5%

27MHZ_OUT

RV970 DIS@ 0_0201_5%

Crystal
GND2 OUT
IN GND1
YV1 27MHZ_7PF_8Y27000005 DIS@

27MHZ_IN

GPU_XTAL_OUT_R

CV105 DIS@ 6.8P_0402_50V8-D

CV106 DIS@ 6.8P_0402_50V8-D

20160419
Add RV970 to reduce crystal driving level

+3VS_AON

RV129 RV111 RV112 RV113 RV114 RV115 RV116 RV117 RV118 RV119 10K_0402_1%

RV114 DIS@ 499K_0402_1%

Strap0 = H
GC6 enable

STRAP0 STRAP1 STRAP2 STRAP3 STRAP4

UV1Q 13/18 MISC2

ROM_CS_N H6
ROM_SI H5
ROM_SO H7
ROM_SCLK H4
BUFRST_N L2

STRAP0 J2
STRAP1 J7
STRAP2 J6
STRAP3 J5
STRAP4 J3

STRAP0 STRAP1 STRAP2 STRAP3 STRAP4 | NC NC NC NC NC
GK107/GK208 GF117 GM107 | GM108

RV920 10K_0402_1%

MULTI_STRAP_REF0_GND_GPU J1

MULTI_STRAP_REF0_GND

RV124 DIS@ 40.2K_0402_1%

N16P-GX_BGA908

+3VS_VGA

RV101 @ RV102 @ RV106 @ RV105 @ RV103 DIS@ RV107 DIS@ 4.99K_0402_1% 10K_0402_5%

X76@

UV1R 11/18 MISC1

VGA_OVERT# M1
OVERT | GPIO8

THERMDN K4
THERMDP K3

NC NC | I2CB_SCL I2CB_SDA
GF117 | GM107/GM108 GK107/GK208

I2CS_SCL T4
I2CS_SDA T3
I2CC_SCL R2
I2CC_SDA R3
I2CB_SCL R7
I2CB_SDA R6

Test_Point_20MIL TP2 AM10
Test_Point_20MIL TP3 AP11
Test_Point_20MIL TP4 AM11
Test_Point_20MIL TP5 AP12
AN11

JTAG_TCK JTAG_TMS JTAG_TDI JTAG_TDO JTAG_TRST_N

RV144 DIS@ 10K_0402_5%

GPIO0 P6 GC6_FB_EN
GPIO1 M3
GPIO2 L6
GPIO3 P5
GPIO4 P7
GPIO5 L7 VGA_MPWR_ON
GPIO6 M7 VGA_EVENT#
GPIO7 N8
GPIO8 L5 SYS_PEX_RST_MON
GPIO9 M2 VGA_ALERT#
GPIO10 L1 MEM_VREF
GPIO11 M5 VGA_PWM_VID
GPIO12 N3 VGA_PWR_LIM_D
GPIO13 M4 VGA_PSI
GPIO16 R8
GPIO20 P4
GPIO21 P1 GPU_PEX_RST_HOLD

GK107/GK208/GF117 NC

GPIO16 GPIO20 GPIO8 | NC NC NC | GPIO16 NC NC
GK208 | GF117 | GK107 | GM107 GM108

N16P-GX_BGA908

GC6_FB_EN [27]
VGA_MPWR_ON [33]
VGA_PWM_VID [75]
VGA_PWR_LIM_D [67]
VGA_PSI [75]
MEM_VREF [31,32]
GPU_PEX_RST_HOLD

+3VS_VGA

RV127 @ 10K_0402_1%

[75] DGFX_PWRGD

DGFX_PWRGD

RV925 @ 0_0402_5%

RV200 NGC6@ 0_0402_5%

DV101 GC6@

[33,75,80] VGA_ON

VGA_ON

RV143 DIS@ 0_0402_5%

GC6_FB_EN

RV138 GC6@ 0_0402_5%

DAN222MGT2L_VMD3

FB_PWR_EN

FB_PWR_EN [79]

RV926 200K_0402_5%

GC6_FB_EN_GPIO

GC6_FB_EN_GPIO [9]

Connect to EC or PCH to indicate the GC6 status of GPU to the system

+3VS_AON

CV109 @ 0.1U_0402_10V6-K

QV102 @ 2N7002KW_SOT323-3

GC6_FB_EN

GC6_FB_EN_D

RV141 DIS@ 0_0402_5%

GC6_FB_EN_GPIO

VGA_PEX_RST#

GPU Thermal shut down pin, sent to EC to control SLP_S3#

[57] WRST#

WRST#

QV22 @ 2N7002W-T/R7_SOT323-3

VGA_OVERT#

CV112 @ 0.01U_0402_25V7-K

20160303
Correct VGA_OVERT# netname and unstuff QV22

+3VS_AON

RV120 DIS@ 2.2K_0402_5%

RV121 DIS@ 2.2K_0402_5%

+3VS_AON

QV21B 2N7002KDWH_SOT363-6 DIS@

EC_SMB_CK3

[11,57,59,62]

QV21A 2N7002KDWH_SOT363-6 DIS@

EC_SMB_DA3

[11,57,59,62]

SMBUS to EC for Thermal

+3VS_AON

VGA_MPWR_ON 1 2 RV130 DIS@ 10K_0402_1%

SYS_PEX_RST_MON 1 2 RV123 @ 10K_0402_1%

VGA_OVERT# 1 2 RV122 DIS@ 10K_0402_1%

VGA_ALERT# 1 2 RV131 DIS@ 10K_0402_1%

VGA_PWR_LIM_D 1 2 RV132 DIS@ 100K_0402_5%

VGA_PSI 1 2 RV133 DIS@ 10K_0402_1%

GPU_PEX_RST_HOLD 1 2 RV134 DIS@ 10K_0402_1%

VGA_EVENT# 1 2 RV135 DIS@ 10K_0402_1%

GC6_FB_EN 1 2 RV146 DIS@ 10K_0402_1%

MEM_VREF 1 2 RV136 DIS@ 100K_0402_5%

VGA_PWR_LIM_D DIS@ 2 DV102 1 RB751V-40_SOD323-2 VGA_PWR_LIM

VGA_PWR_LIM [57]

VGA_ALERT# 2 DV103 1 RB751V-40_SOD323-2 @

+3VS_AON

UV101 GC6@

1 B VCC 5
2 A
3 GND Y 4

74LVC1G08GW_SOT353-1-5

SYS_PEX_RST_MON

VGA_PEX_RST#

VGA_PEX_RST# [25]

RV128 GC6@ 0_0402_5%

NGC6@ RV140 1 2 0_0402_5% SYS_PEX_RST_MON_R

+3VS_AON

UV102 DIS@

5 VCC B 1
A 2
4 Y GND 3

74LVC1G08GW_SOT353-1-5

SYS_PEX_RST_MON_R

DGPU_HOLD_RST#

PLT_RST#

[12,42,48,49,56,57,58]

GPIO from PCH

+3VS_AON

CV110 DIS@ 0.1U_0402_10V6-K

QV101 DIS@ 2N7002KW_SOT323-3

VGA_EVENT#

GPU_EVENT#_R

RV147 DIS@ 0_0402_5%

RV145 @ 0_0402_5%

GPU_EVENT#

GPU_EVENT# [11]

PCH GPIO Pin to wake up GPU from GC6

X76

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16P-GT	Samsung	K4G41325FE-HC28	PD 45.3K	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5GC4H24AJR-T2C 256X16	PD 34.8K							
	Micron	EDW4032BABG-60-F 256X16	PD 24.9K							

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR	Samsung	K4G80325FB-HC03	PD 4.99K	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5GC8H24MJR-T2C	PD 30.1K							
	Micron	MT51J256M32HF-60:A	PD 10K							

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Title: 034_N16P-Q1/Q3(4/6): GPIO

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

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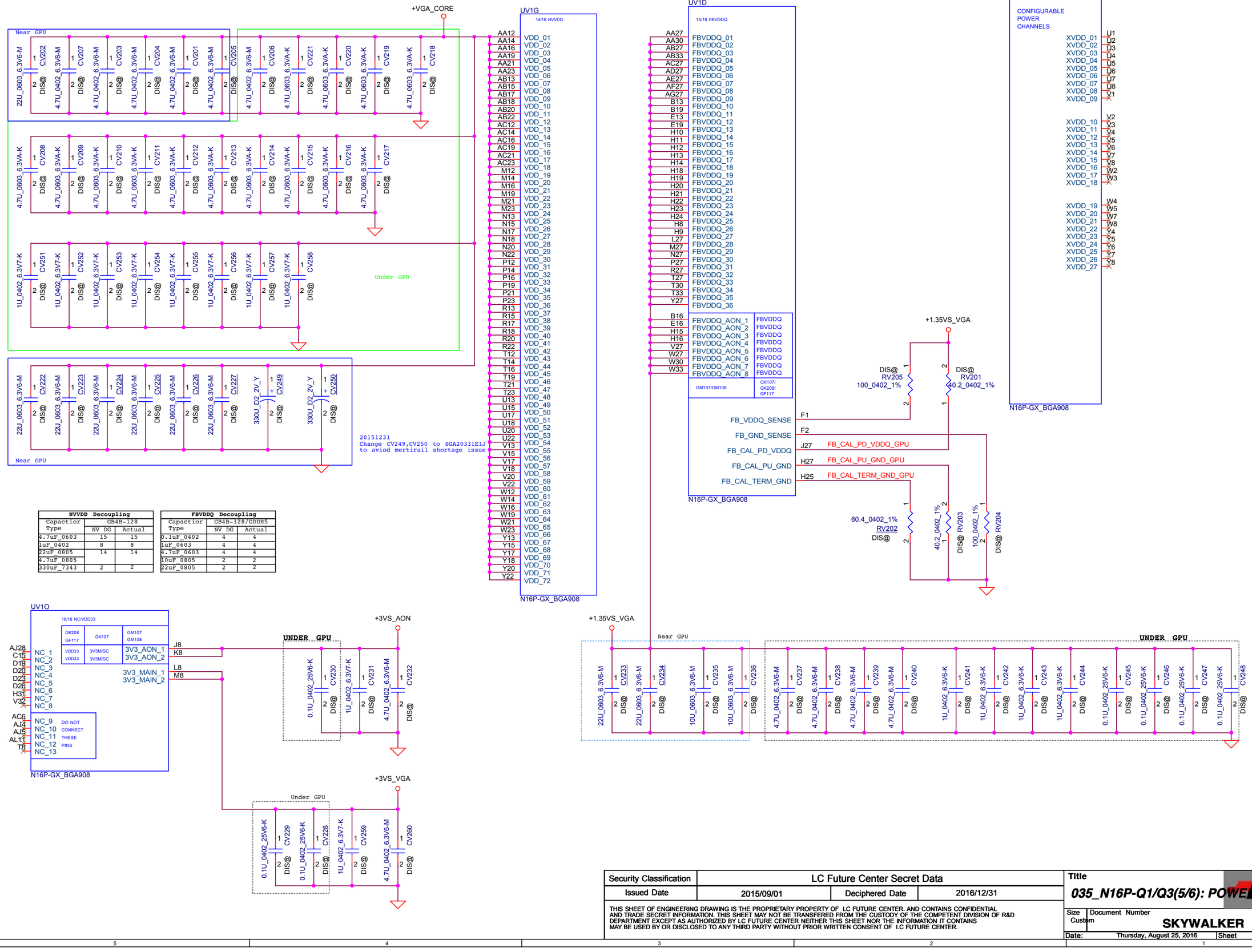

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: *035_N16P-Q1/Q3(5/6): POWE*

Size	Document Number	Rev
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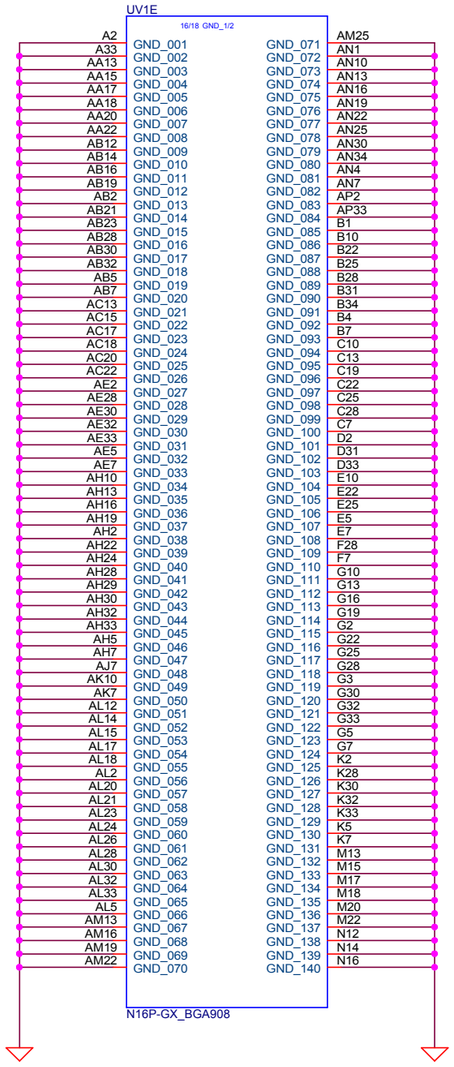

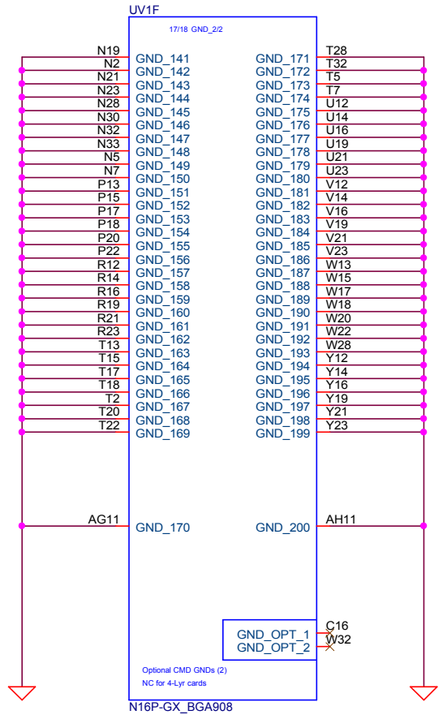

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: *036_N16P-Q1/Q3(6/6): GND*

Size	Document Number	Rev
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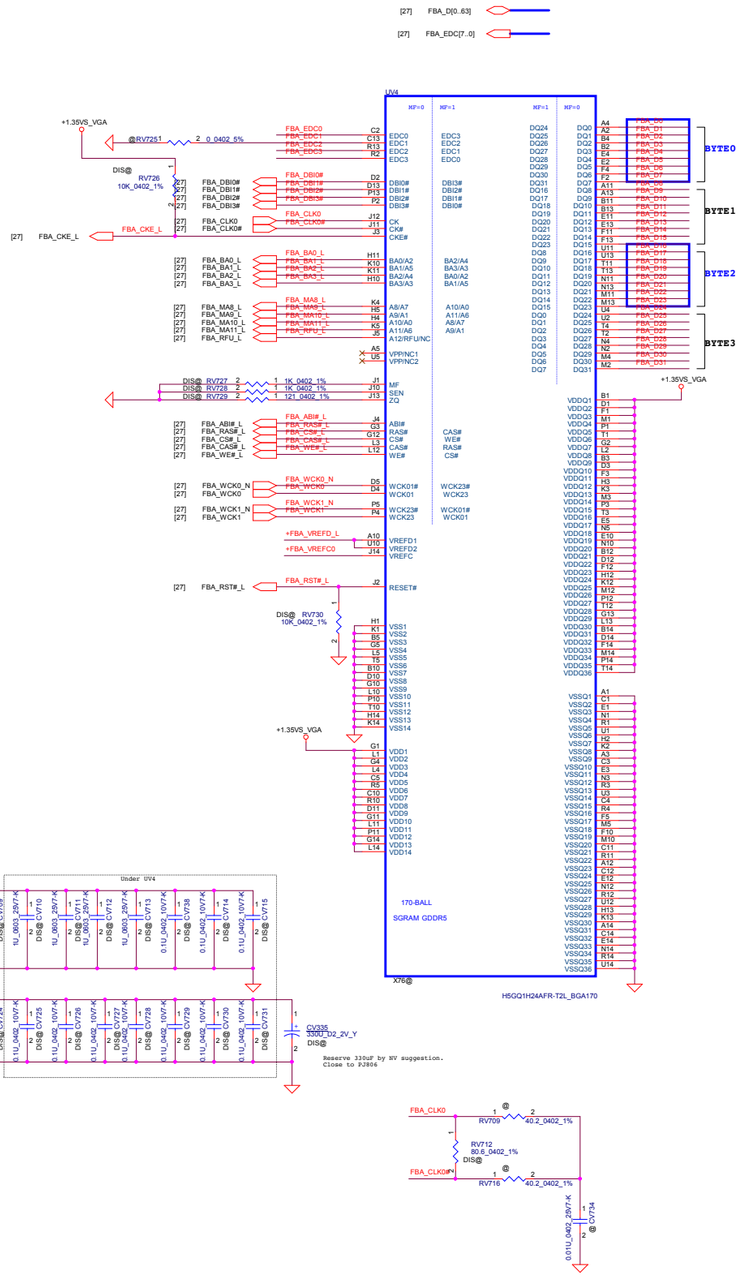

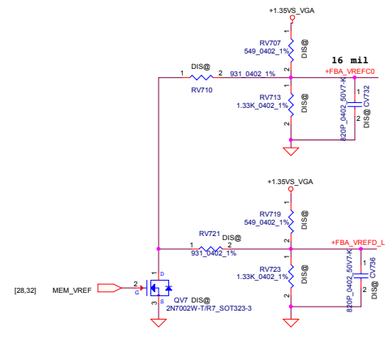

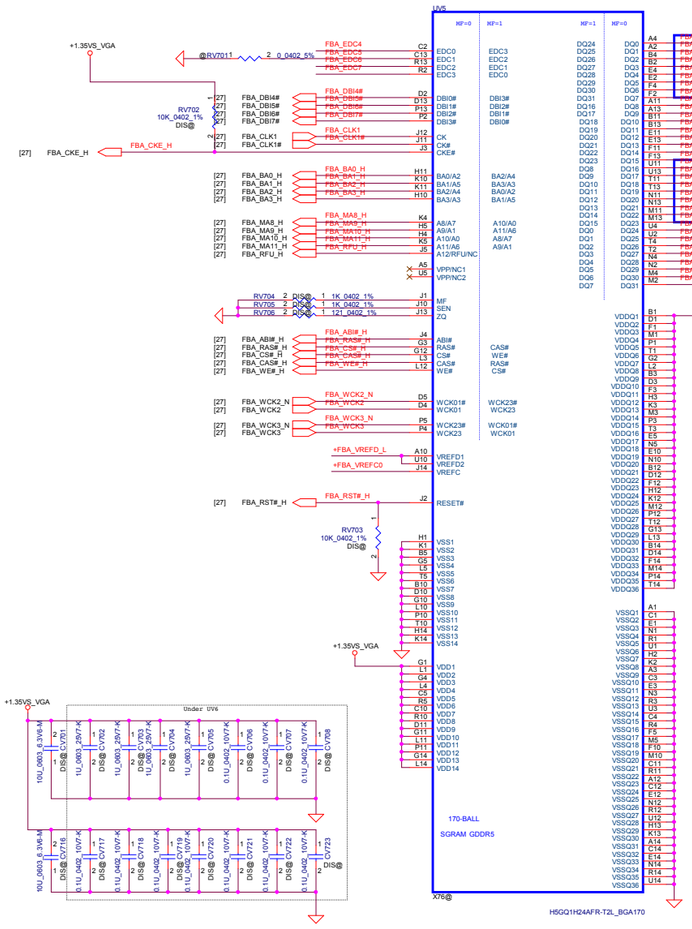

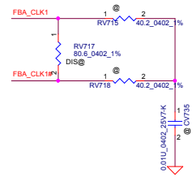

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Title: VRAM CH_A

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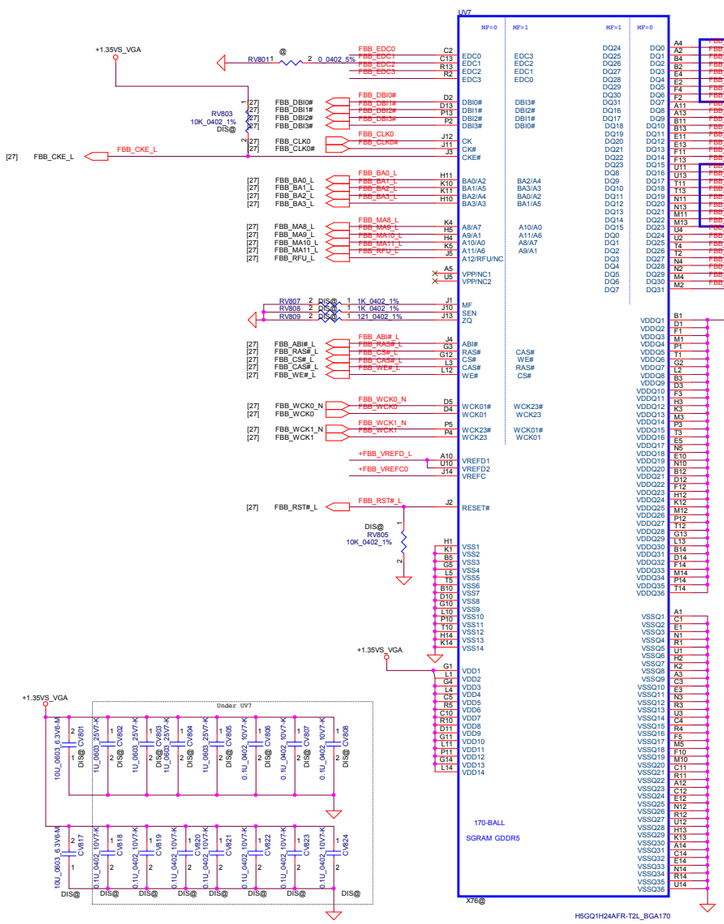
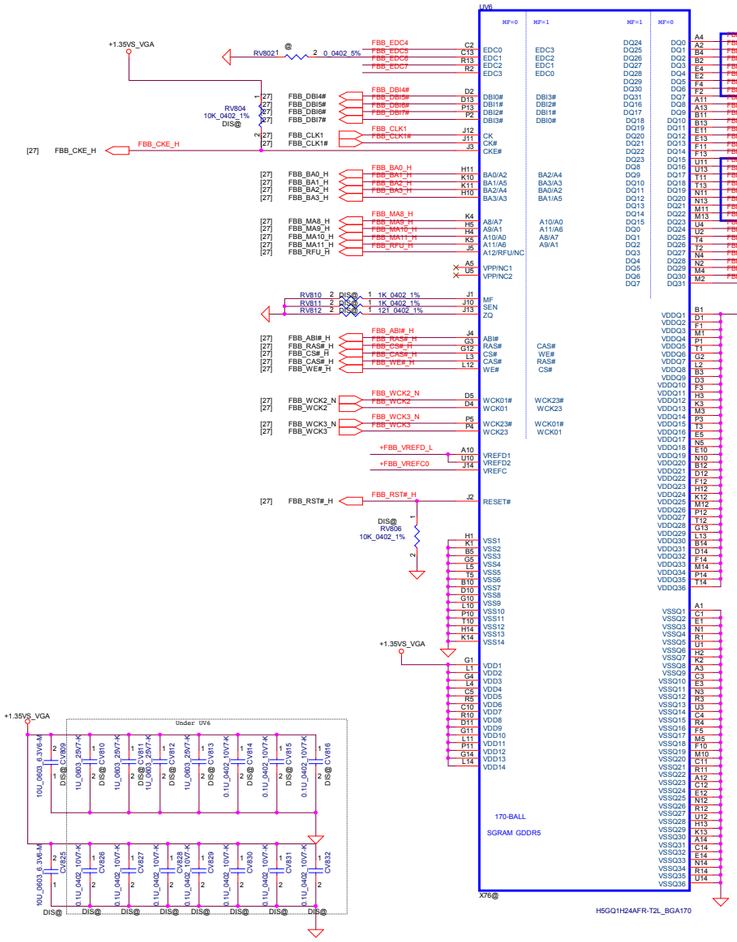
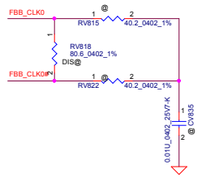
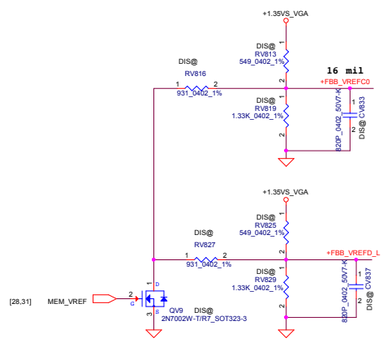
[27] FBB_D[0..63]

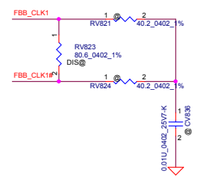
[27] FBB_EDC[7..0]











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Title: VRAM CH_B

Size	Document Number	Rev
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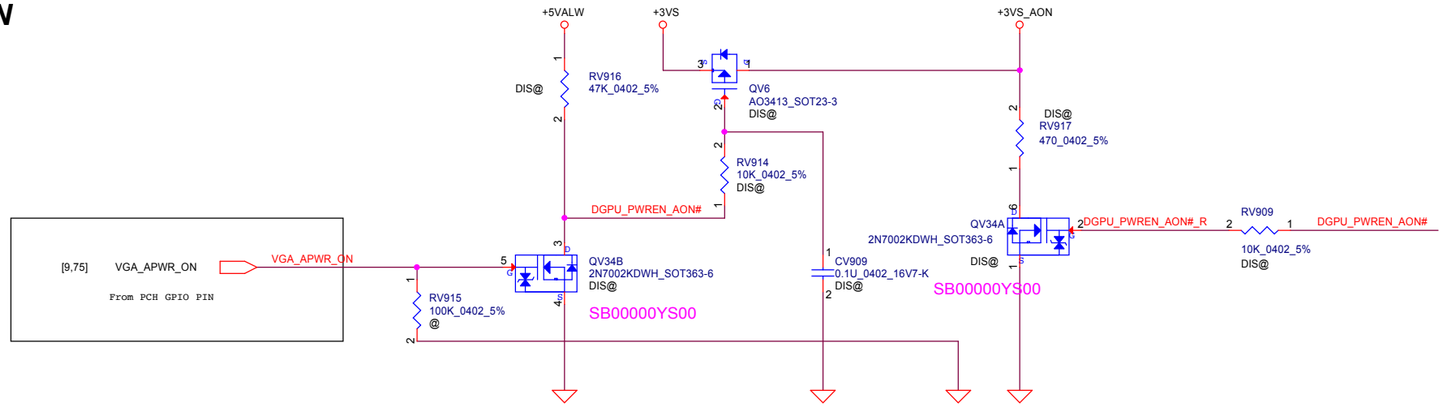
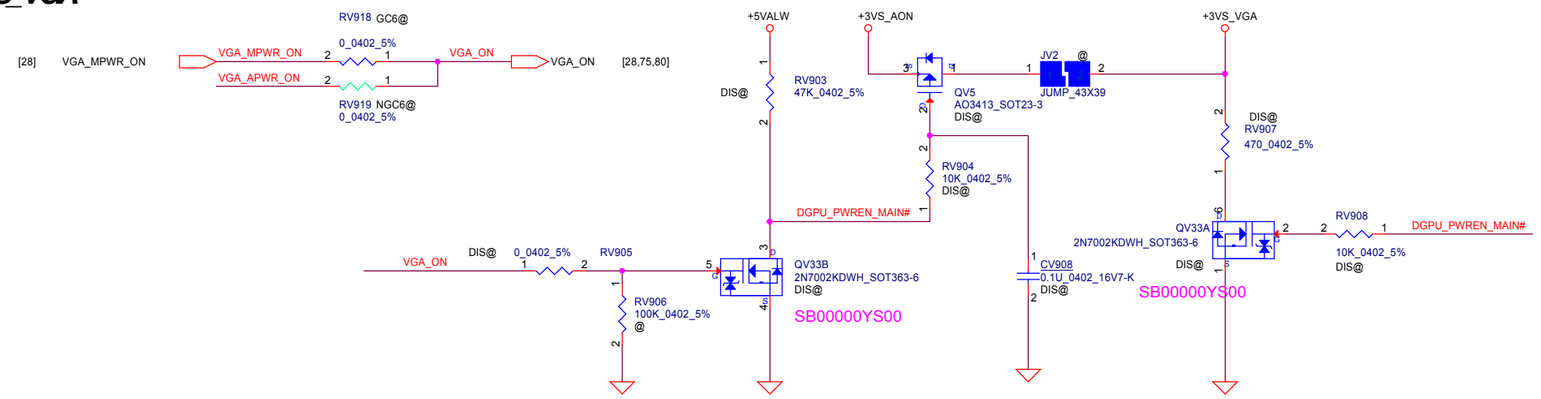
+3VS to +3VS_AON

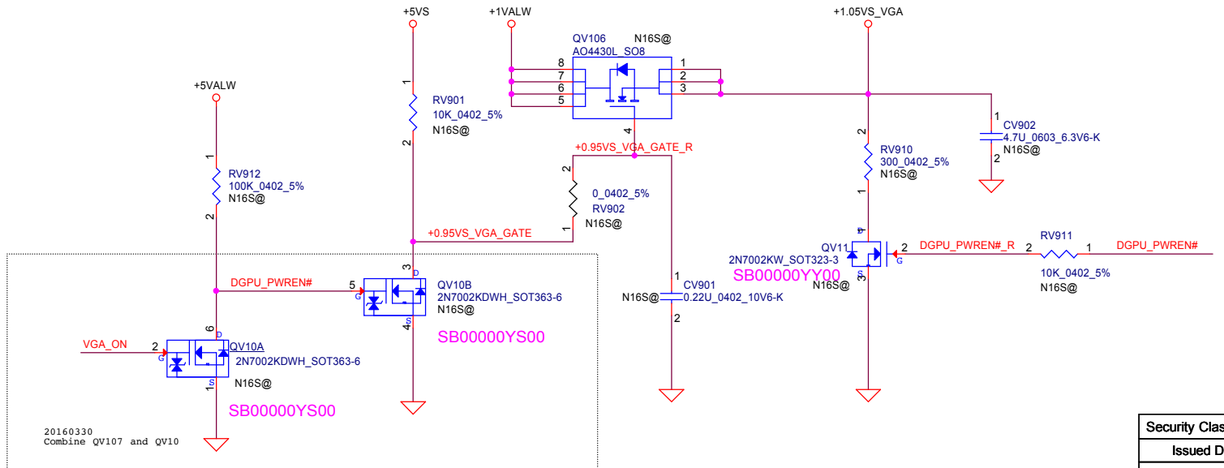


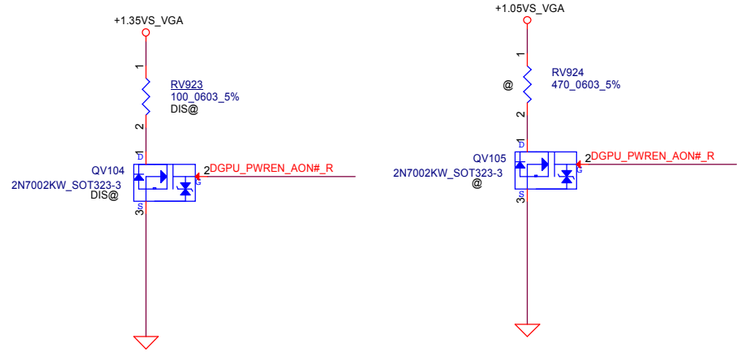
+3VS_VGA



20160310
Add 1.05VS_VGA circuit for N16S GPU

+1VALW to +1.05VS_VGA





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Title: *N16S-GT swich power*

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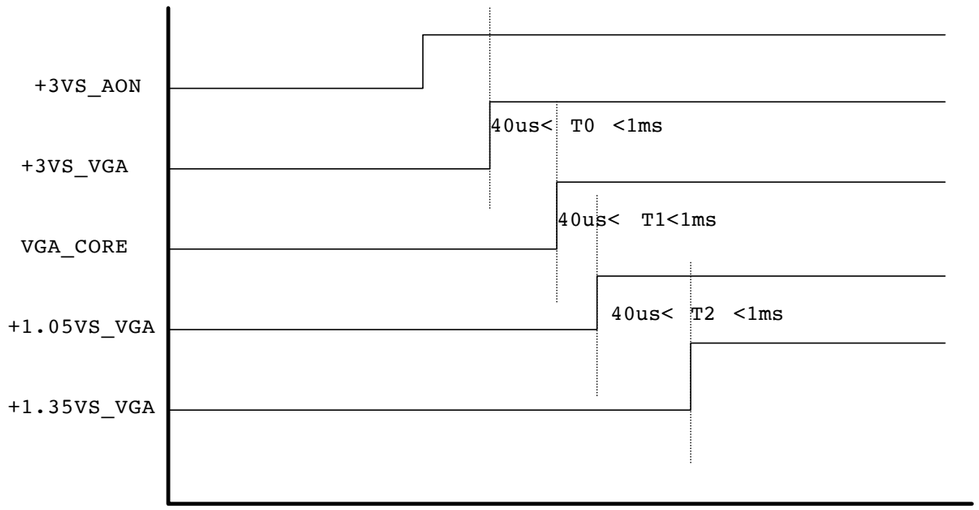
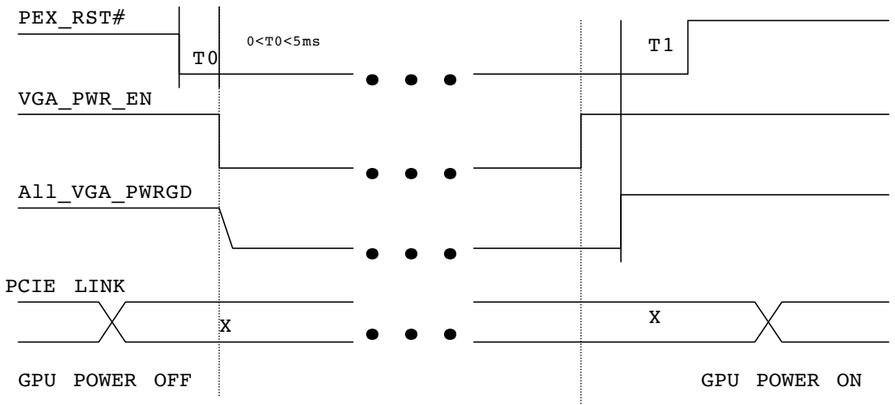
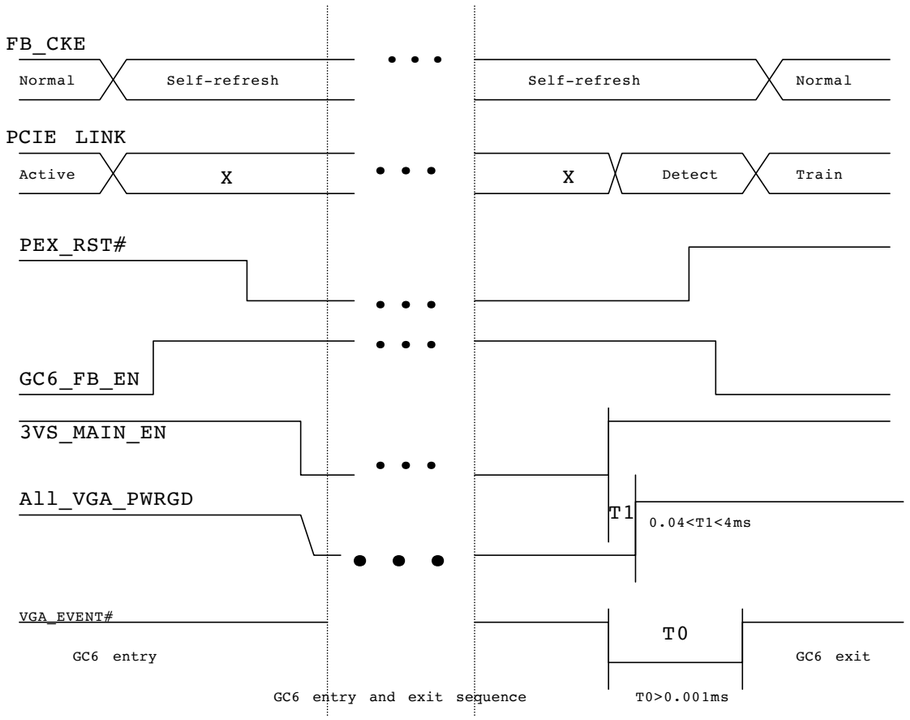
GPIO	I/O	Functional Description	I/O Termination
GPIO0	O	FB Enable for GC6 2.0, Open source	10K pull-down
GPIO1	O	Memory voltage control	Pull-up/pull down to set the FBVDD/Q boot voltage
GPIO2	O	Panel Backlight PWM Brightness Control	100K pull down
GPIO3	O	Panel Power Enable	100K pull down
GPIO4	O	Panel Backlight Enable	100K pull down
GPIO5	O	GPU Power Sequence for GC6 2.0, Open Drain	10k pull-up to 3V3_AON
GPIO6	I	GPU wake signal for GC6 2.0	10k pull-up to 3V3_AON
GPIO7	O	3D Vision L/R signal	100K pull down
GPIO8	O	System side PCIe rest monitor	10k pull-up to 3V3_AON
GPIO9	I/O	Active low thermal alert, open drain	10k pull-up to 3V3_AON
GPIO10	O	Memory VREF Control	100K pull down
GPIO11	O	GPU Core VDD PWM control signal	
GPIO12	I	AC power detect or power supply overdraw input	100k pull-up to 3V3_AON
GPIO13	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase
GPIO14	I	Hot Plug Detect for IFPA used as DisplayPort for IFPAB when used as Dual Link DVI	
GPIO15	I	Hot Plug Detect for IFPC	
GPIO16	I	Active Low Frame Lock, Open Drain	10k pull-up to 3V3_AON
GPIO17	I	Hot Plug Detect for IFPD	
GPIO18	I	Hot Plug Detect for IFPE	
GPIO19	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	
GPIO20	O	Reserved	
GPIO21	O	GPU PCIe self-reset control, Open Drain	10k pull-up to 3V3_AON
OVERT	I/O	Catastrophic Over Temperature	100k pull-up to 3V3_AON





Optimus entry and exit sequence



GC6 entry and exit sequence

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Title: **P35-GPU GPIO table & sequence**

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Title: *Blank*

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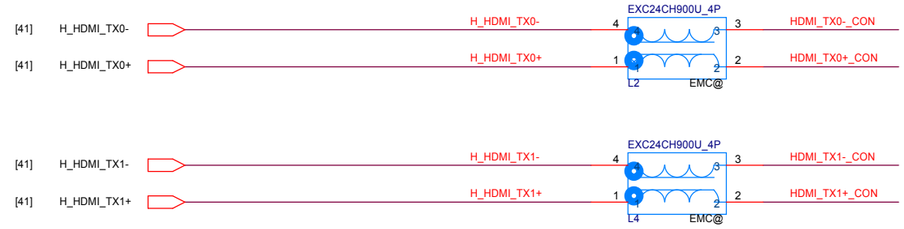
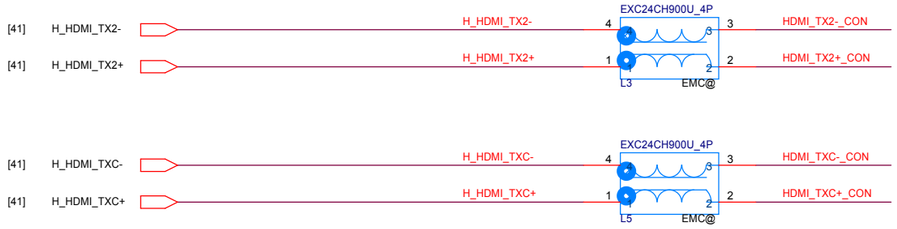
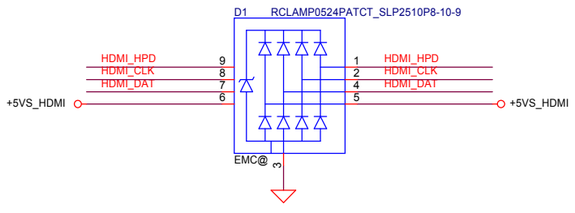
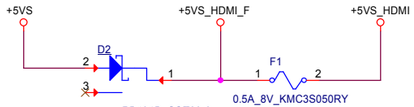
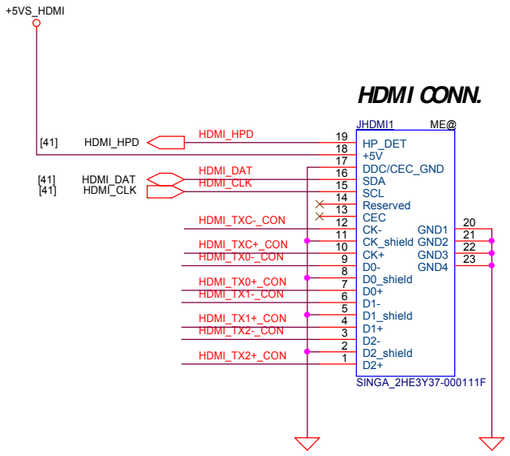


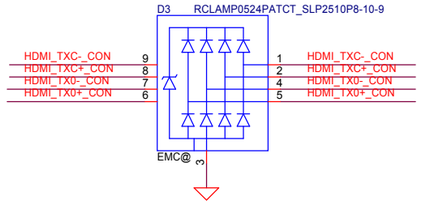


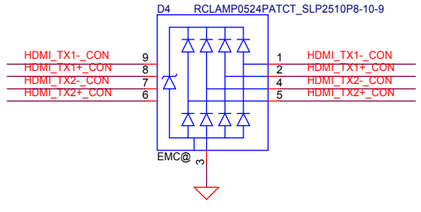


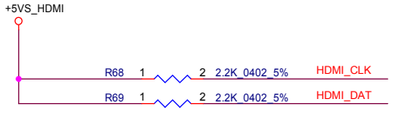




HDMI CONN.







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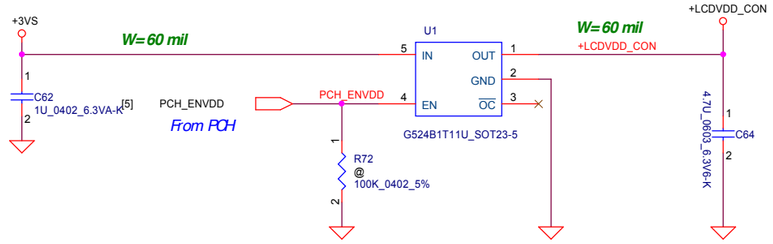
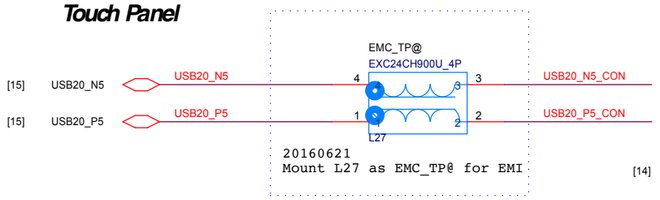
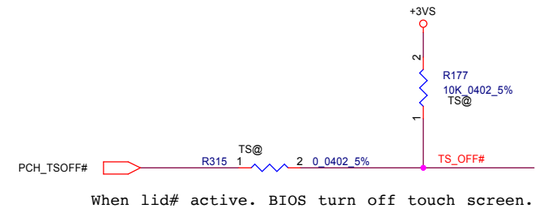
LCDVDD Circuit



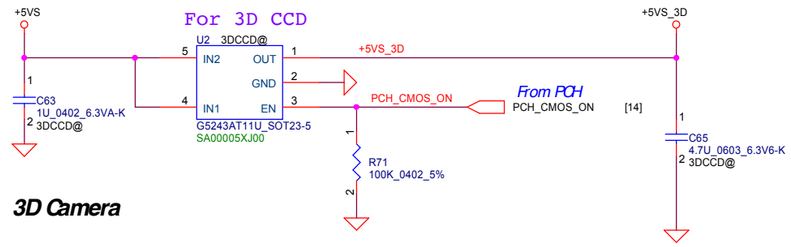
Touch Panel





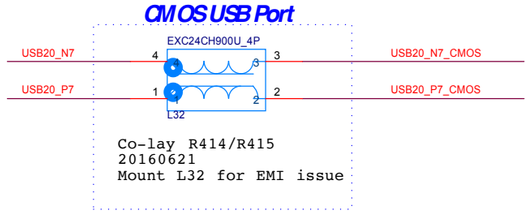
When lid# active. BIOS turn off touch screen.

3D Camera



CMOS Camera

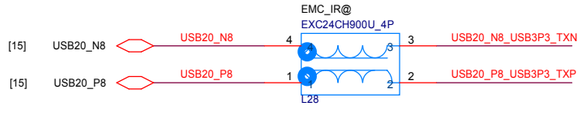
CMOS USB Port



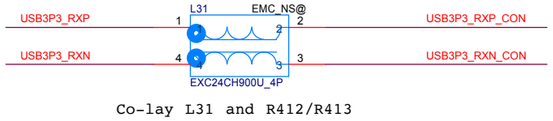
Co-lay R414/R415
20160621
Mount L32 for EMI issue

2D camera module mount choke already

IR camera USB Port

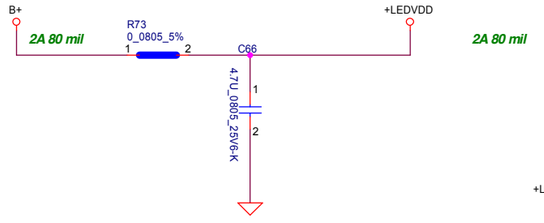


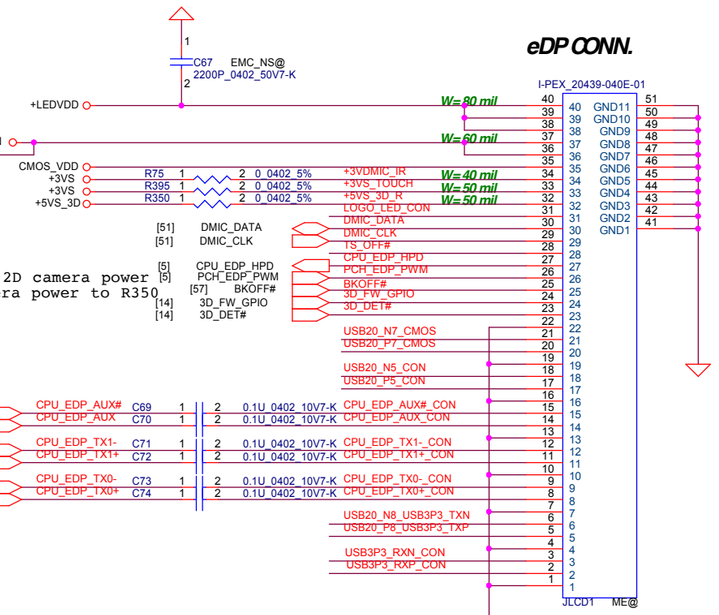
3D CCD USB Port



Co-lay L31 and R412/R413

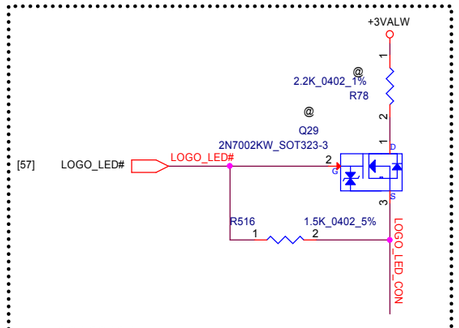
3D camera module mount choke on RX already



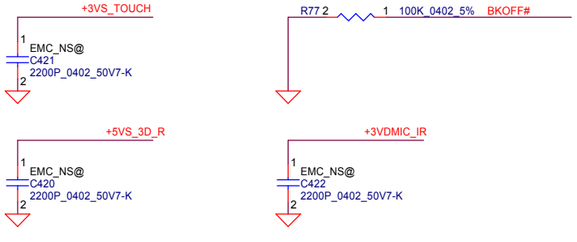


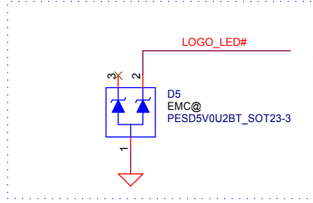
eDP CONN.

20160421
1. Spreate 3D and 2D camera power
2. Connect 3D camera power to R350



20160424
1. Change R516 from 100 to 1.5Kohm for LED brightness





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Title: **eDP CONN**

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Security Classification	LC Future Center Secret Data		
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Title: ***BLANK***

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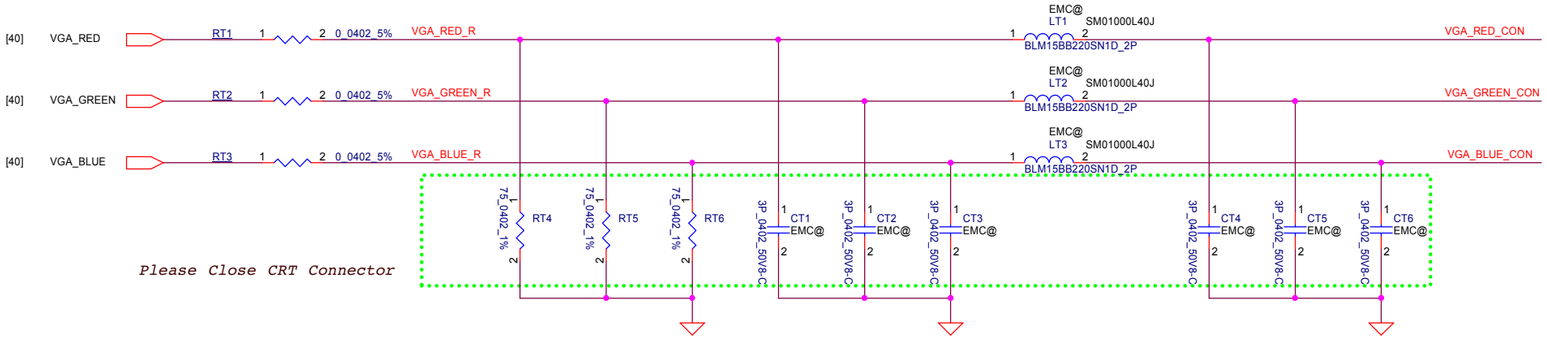
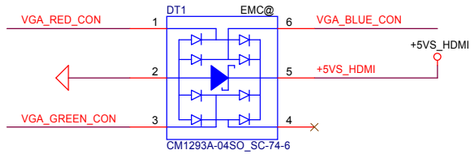
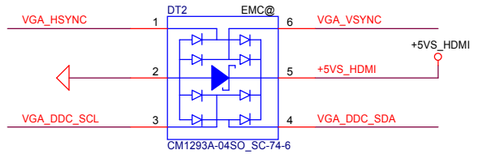
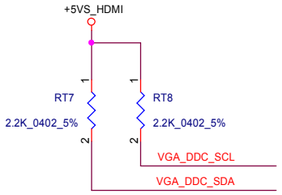


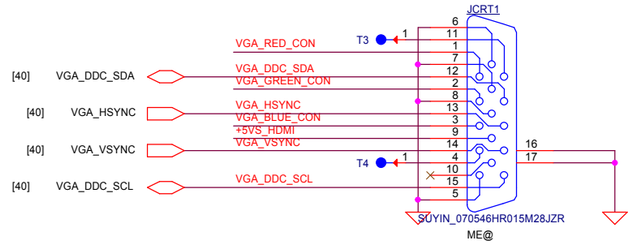






Only for 15'

CRT Connector



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Title: CRT CONN

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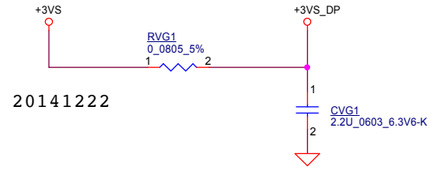
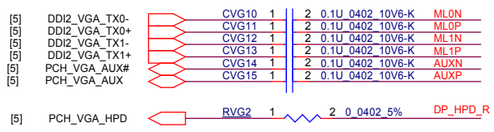
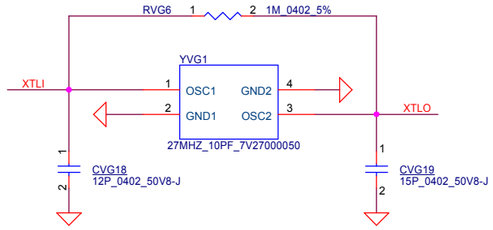
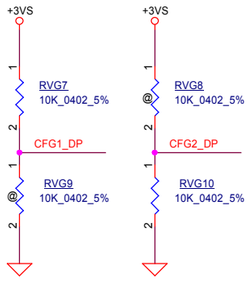






20160127
Change CVG19 to 15p by vender suggestion



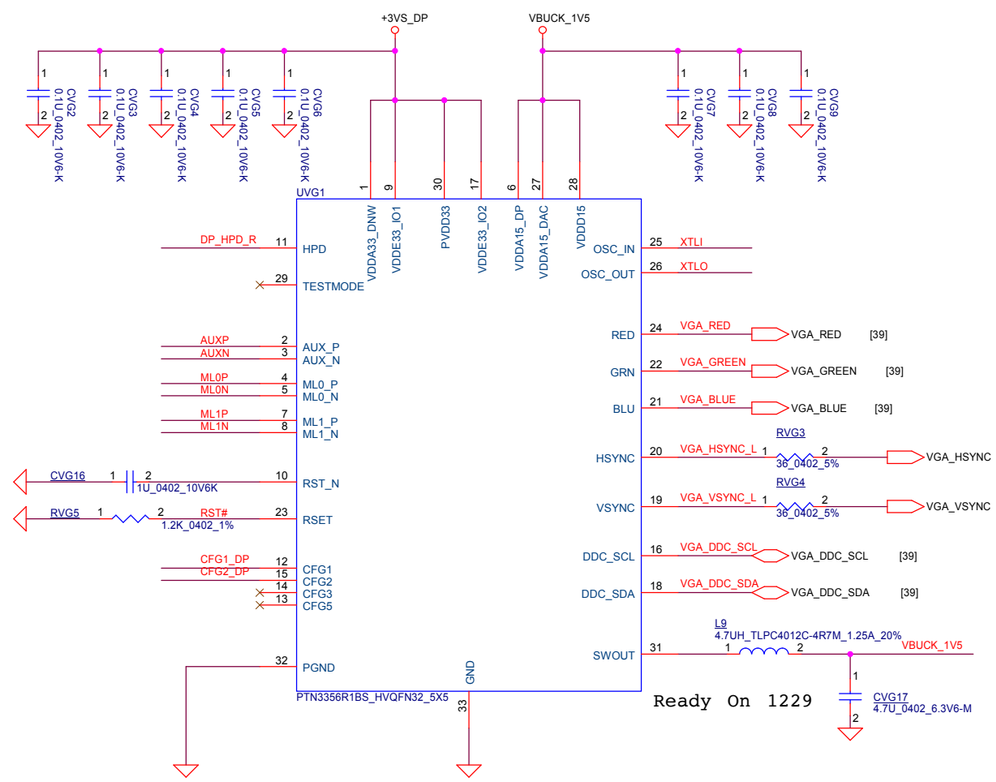


Table 7. CFG1/CFG2 pin definitions

Pin value	System behavior
00	Compliant HPD behavior
01	Most interoperable (non-compliant) HPD behavior
10	Most interoperable (non-compliant) HPD behavior
11	(Default) Compliant behavior

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Title: DP to VGA

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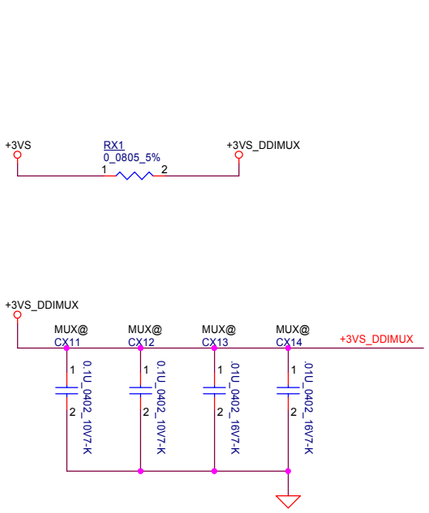
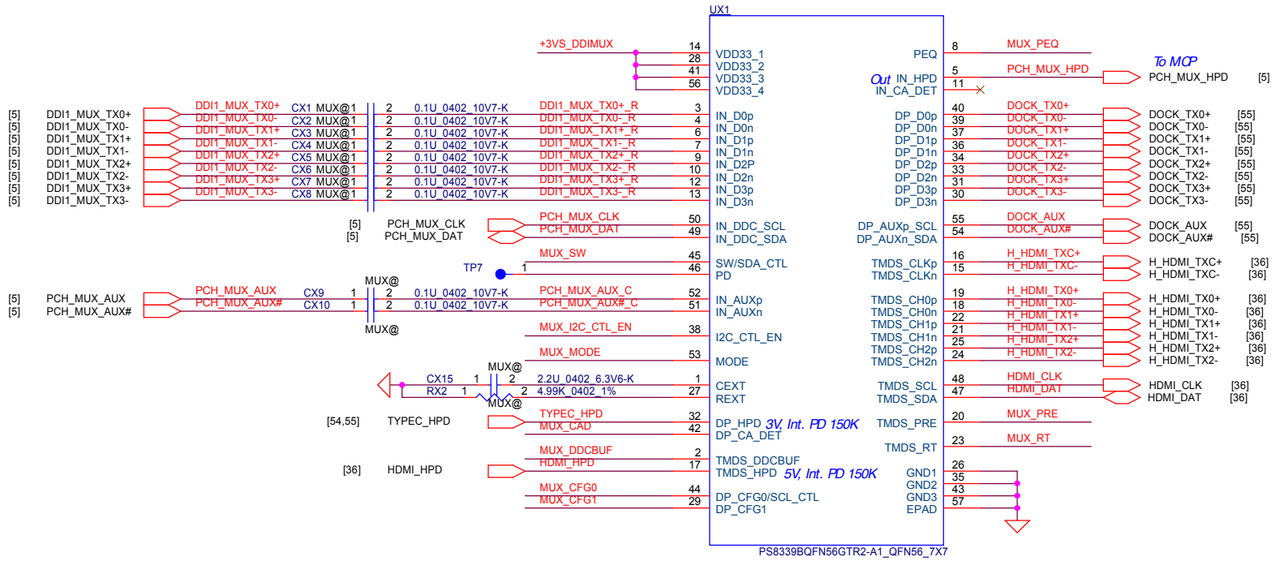
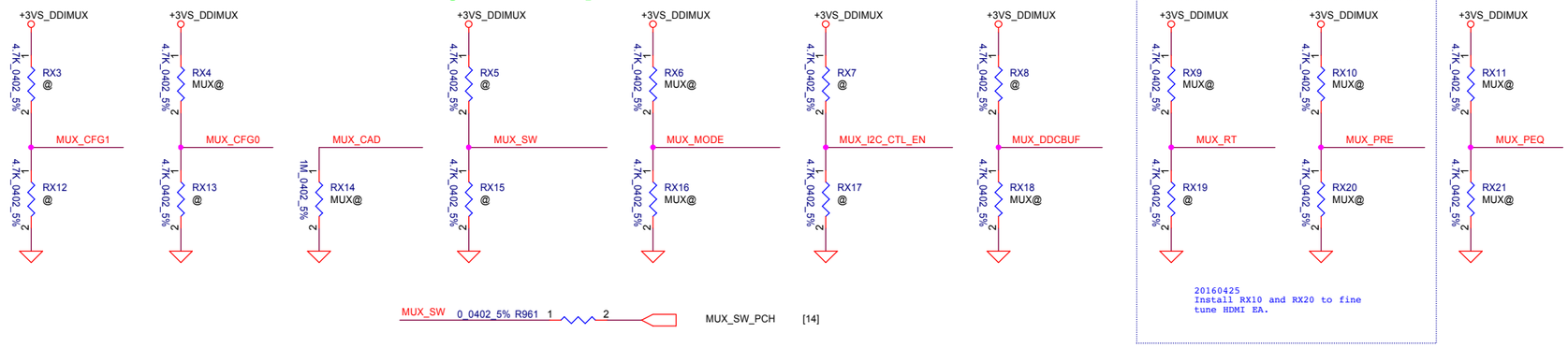




Auto Mode
DP Higher Priolity

Pass Through Mode



20160419
1. Connect MUX_SW to PCH, display priolity control by BIOS
2. Add R961 0 ohm and unstaff RX15.

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Title: **Mux IC**

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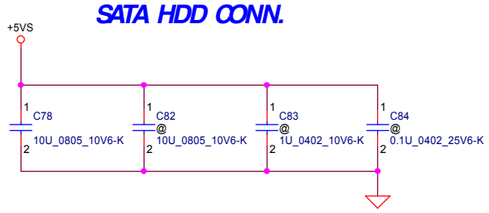
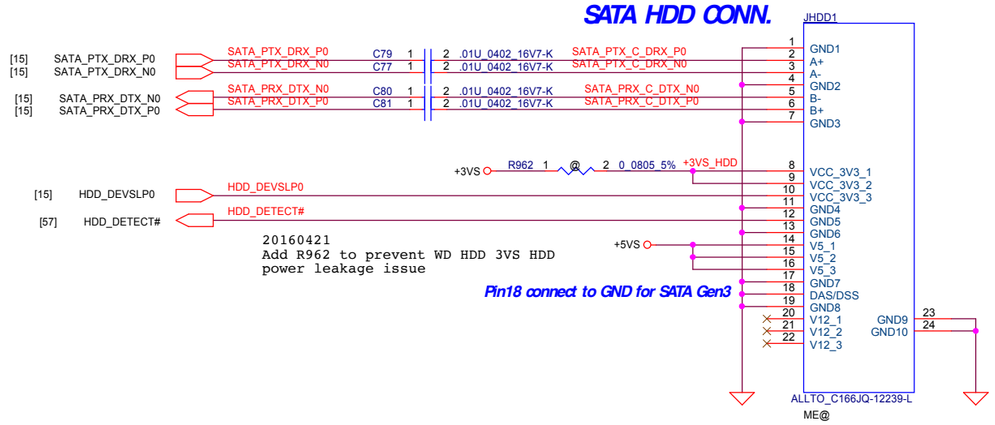
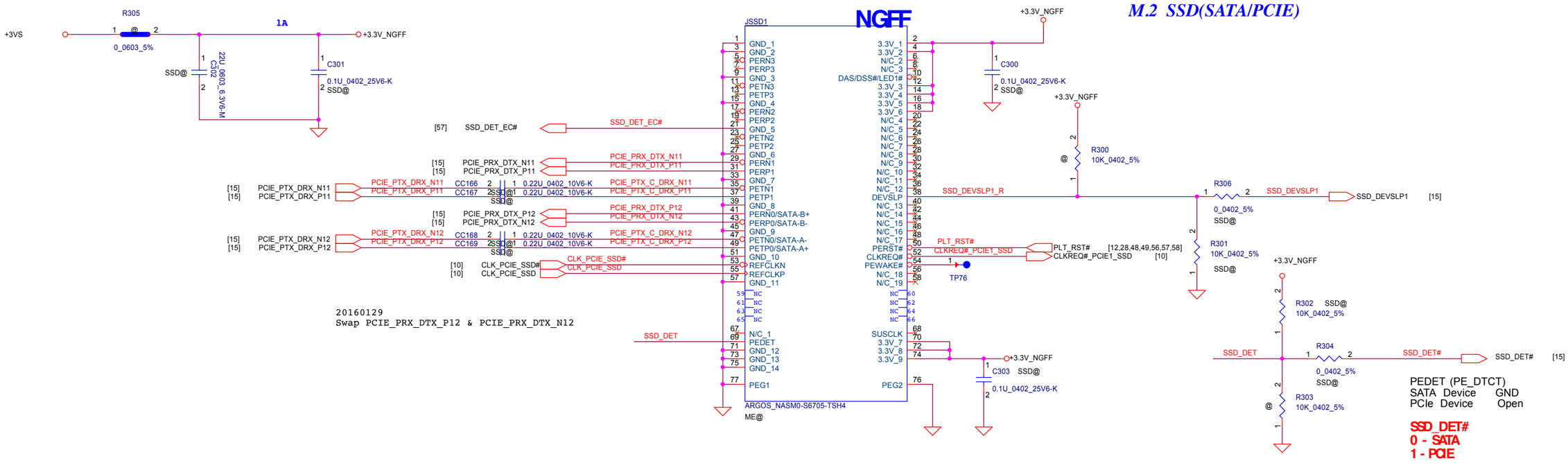
SATA HDD CONN.



SATA HDD CONN.



M.2 SSD(SATA/PCIE)



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Title: **SATA HDD**

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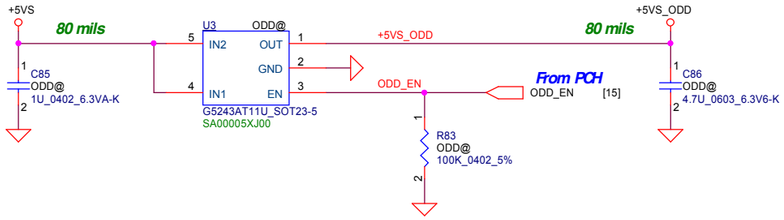
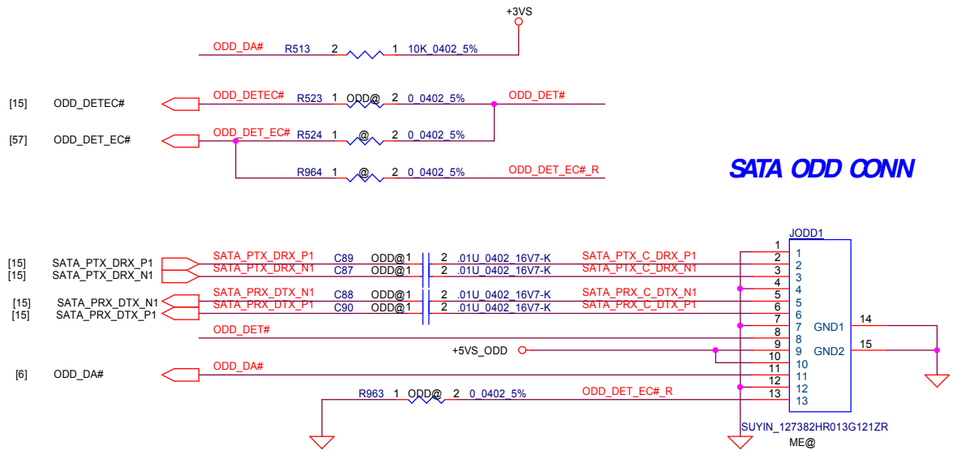
+5VS TO +5VS_ODD





SATA ODD CONN

20160421
Add R963 and reserve R964 for tember function

Title			
ODD			
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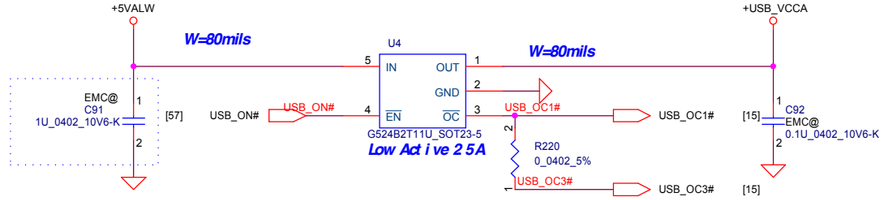
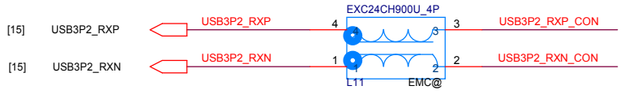
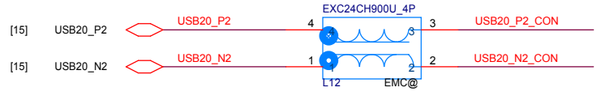
USB3 PORT2

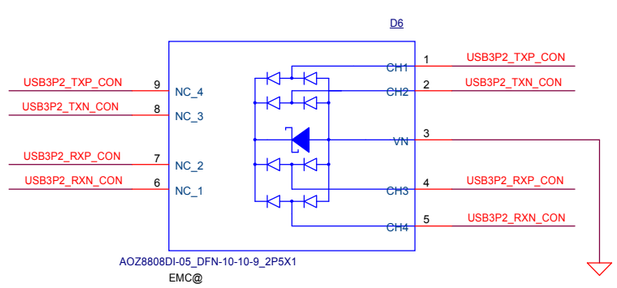
POWER SWITCH

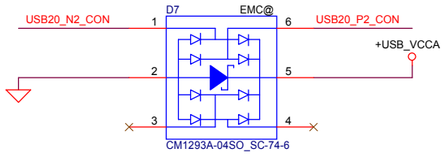


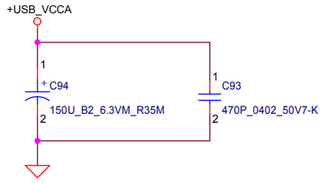
20160616
Change C91 for 0.1U_0402_10V6-K to 1U_0402_10V6-K EMC@

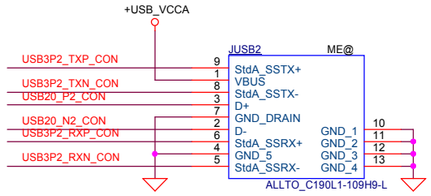




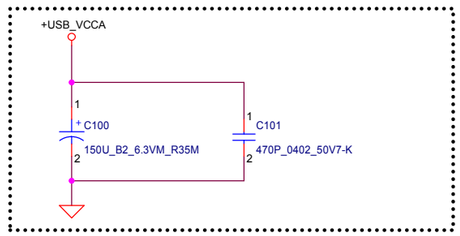


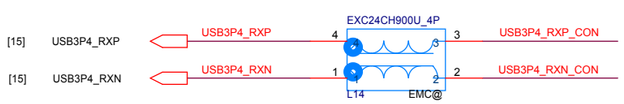


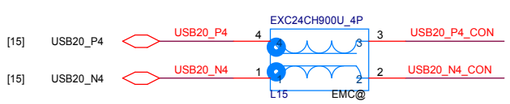


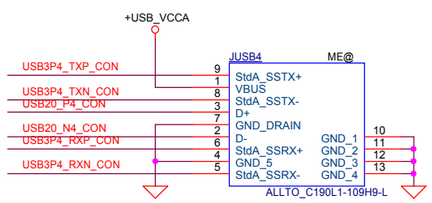


PORT4









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Title: **USB3 PORT1/PORT2(AOU)**

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Title: ***GBE LAN PHY***

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Title

RJ45 CONN

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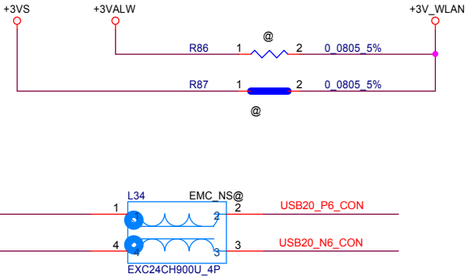
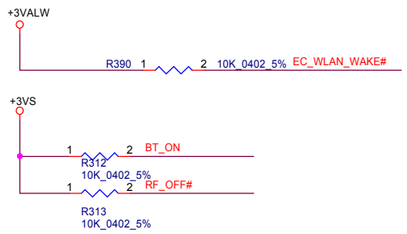
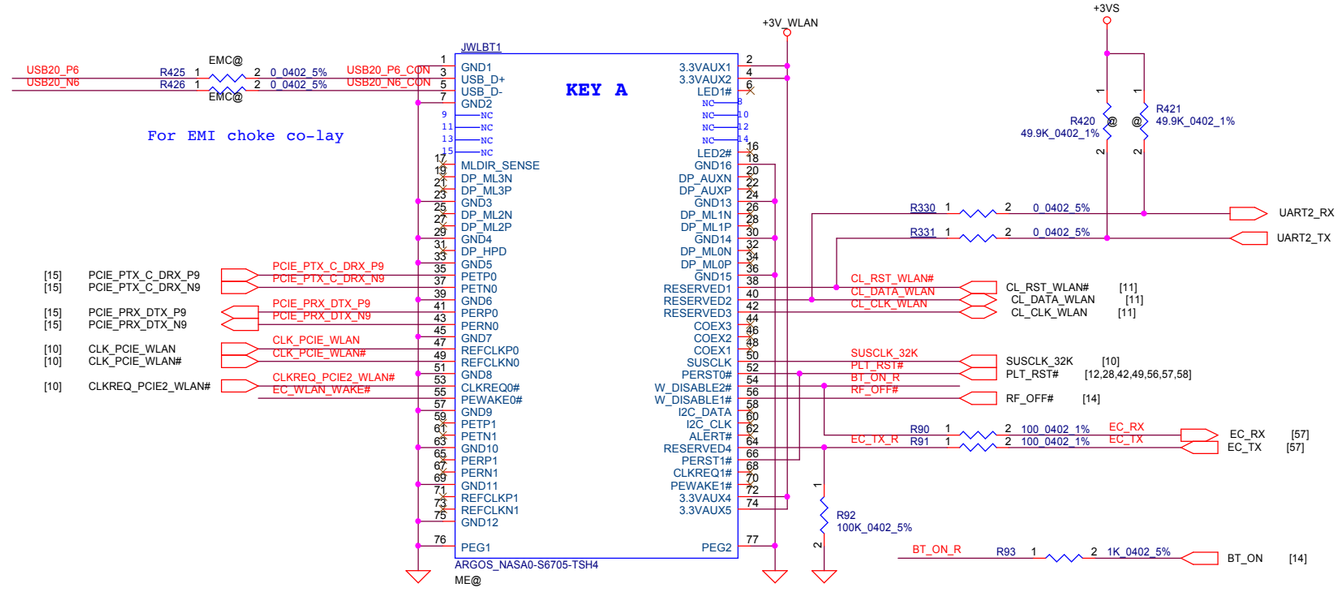
TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR







Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **WWAN/WLAN NGFF CONN.**

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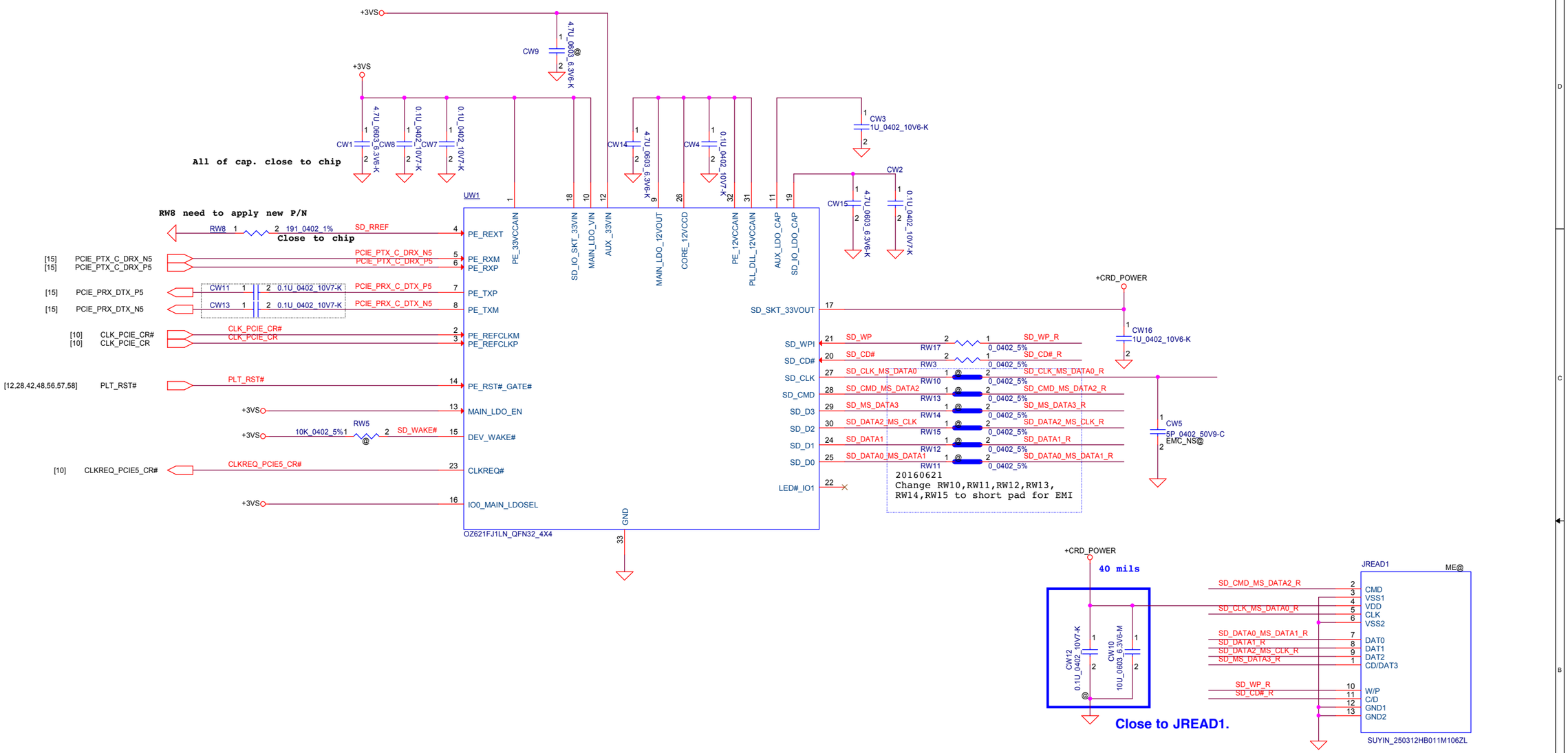

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Title: **Card Reader**

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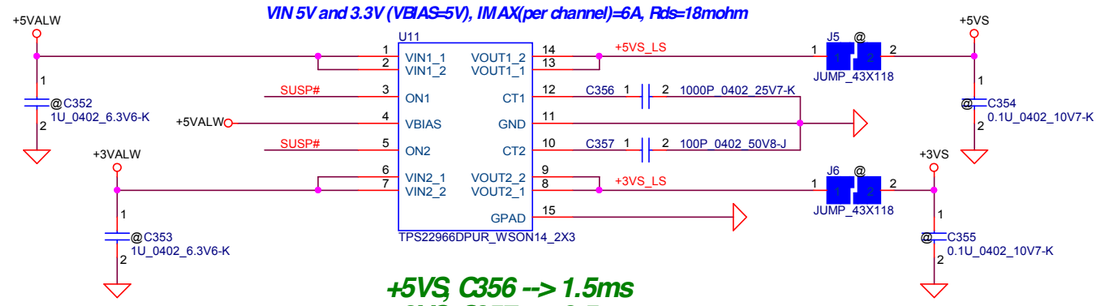
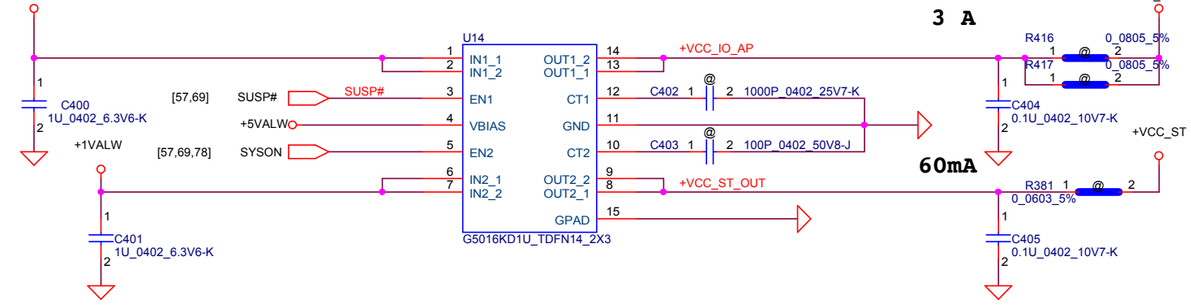
Load Switch
+5VALW To +5VS
+3VALW To +3VS

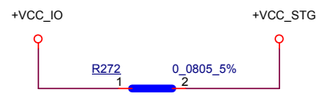


+5VS, C356 --> 1.5ms
+3VS, C357 --> 2.5ms

+1VALW to +VCC_IO_AP & +VCC_ST

Unstaff C402 and C403 for the fastest sequence.





Slew Rate=10uS<TR<65us

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **DC V TO VS/ V-PCH/VM**

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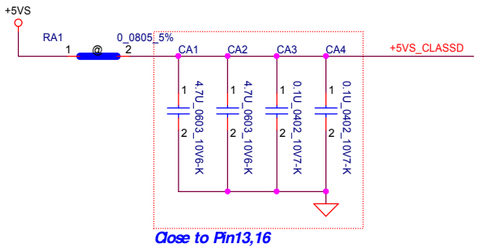
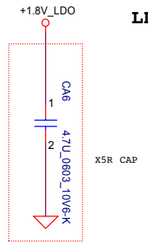
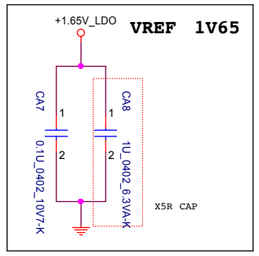




LDO 1V8



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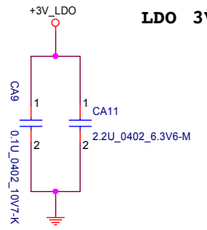
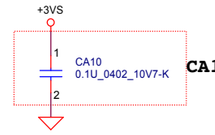
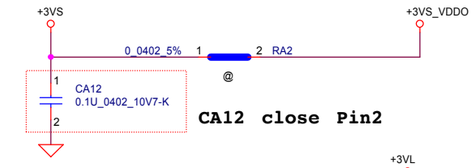


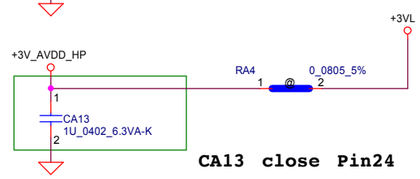
LDO 3V3



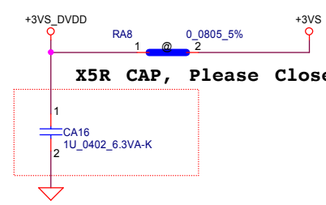
CA10 close Pin7



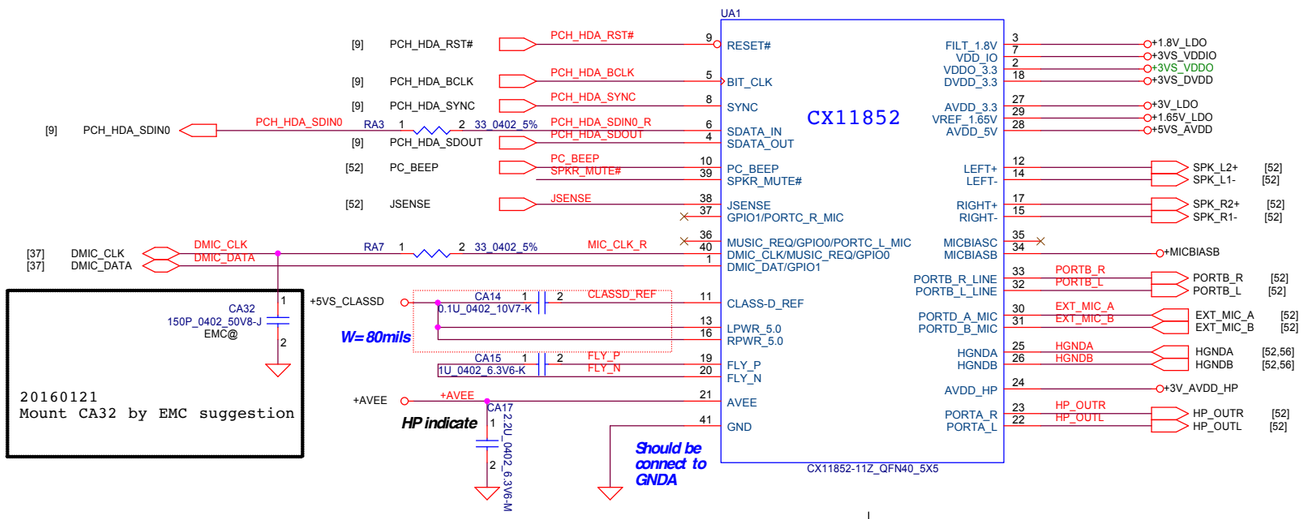
CA12 close Pin2



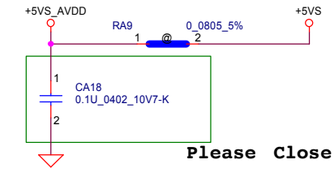
CA13 close Pin24



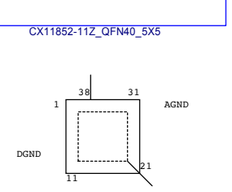
X5R CAP, Please Close Pin18



Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA



Please Close Pin28



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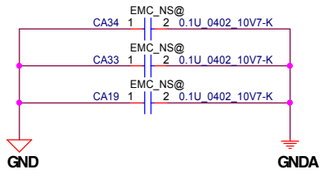

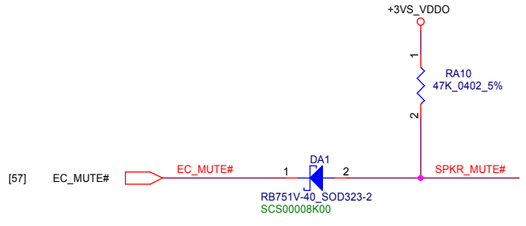

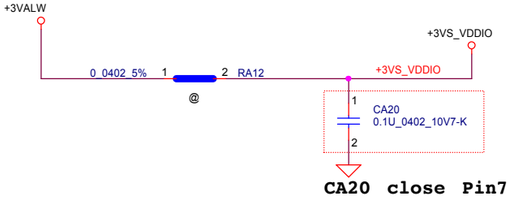

CA20 close Pin7

Title: **Audio Codec**

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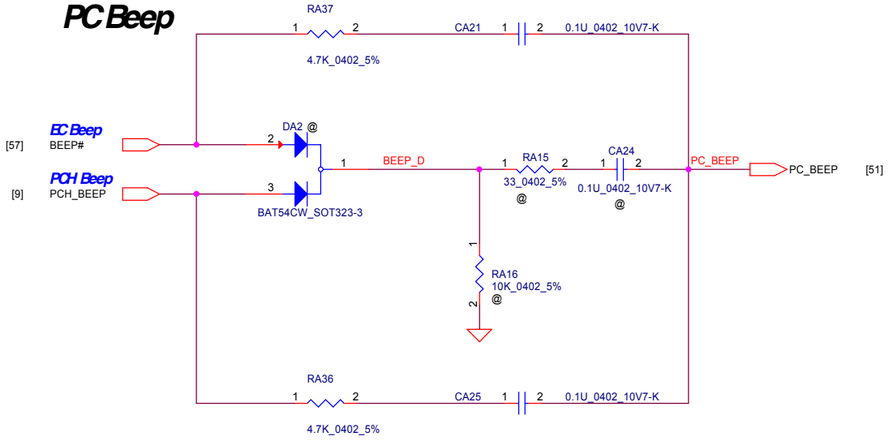
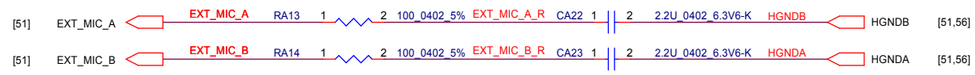
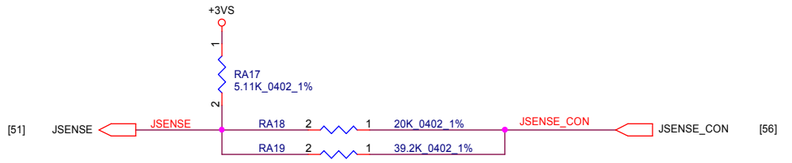
PC Beep



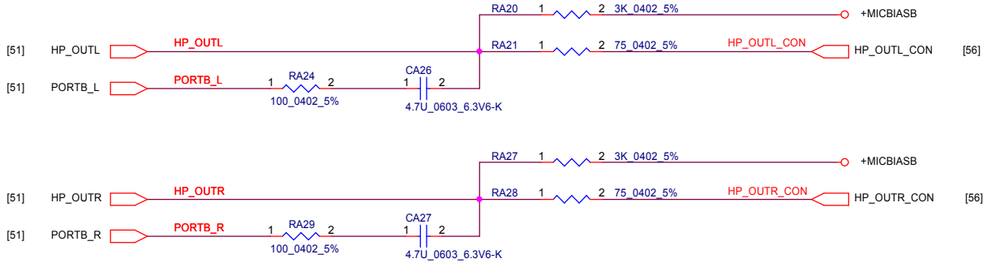
EXT. MIC/ LINE IN

Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA



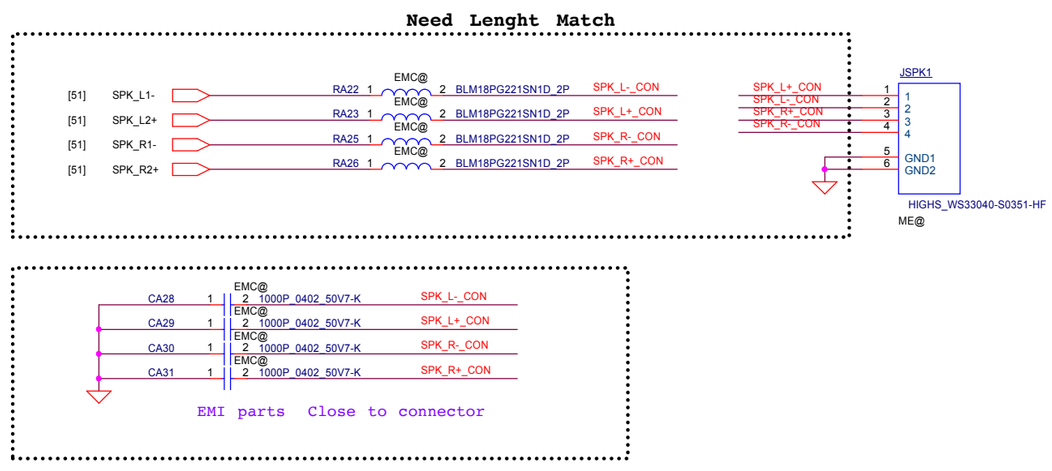


HeadPhone/ LINE OUT



Speaker OUT

SPK CONN.



Title: **HP/MIC JACK/Speaker**

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Security Classification	LC Future Center Secret Data		
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Title: ***BLANK***

Size	Document Number	Rev
Custom	***SKYWALKER***	2.0

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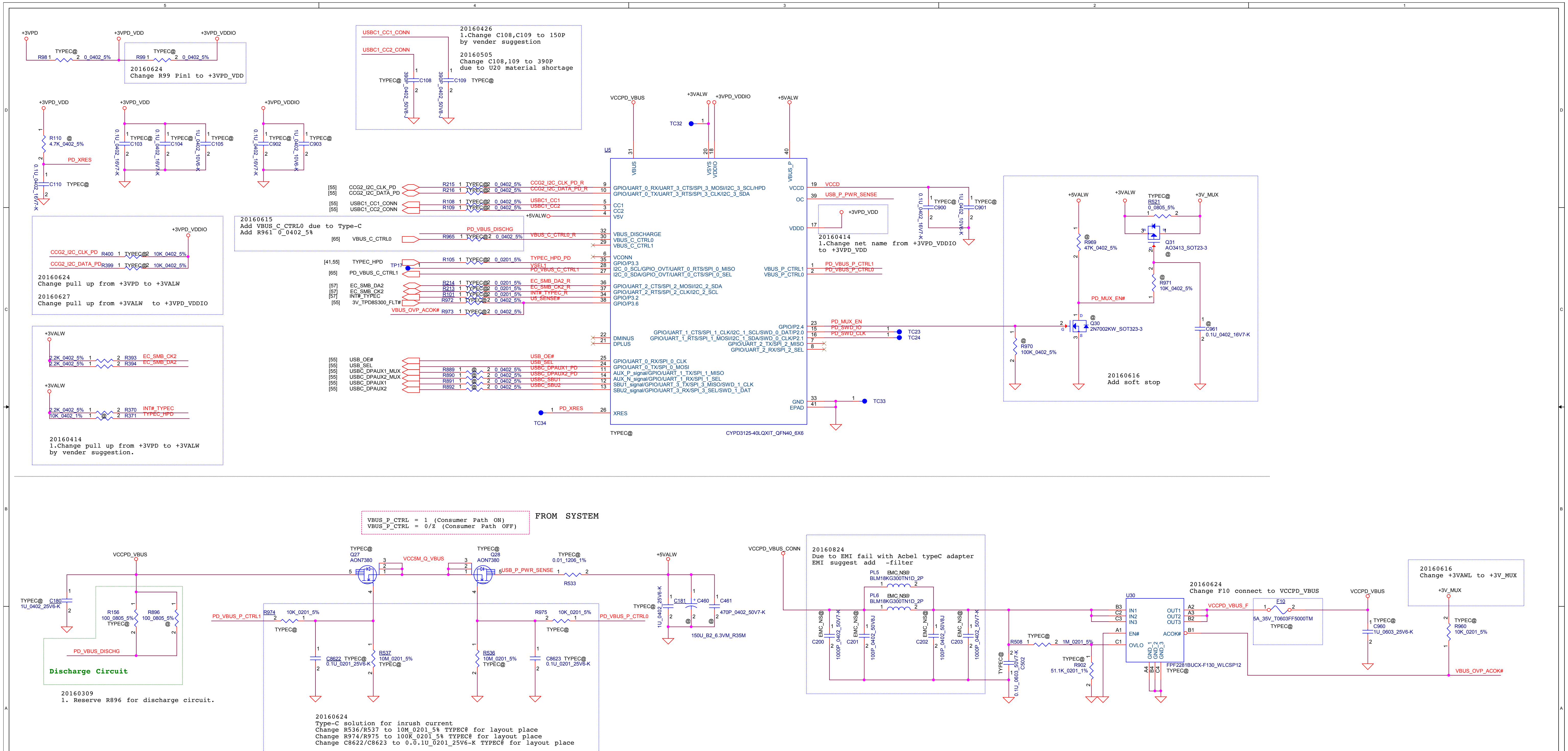

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **TYPE-C_Controller**

Size: Custom | Document Number: KENOBI | Rev: 2.0

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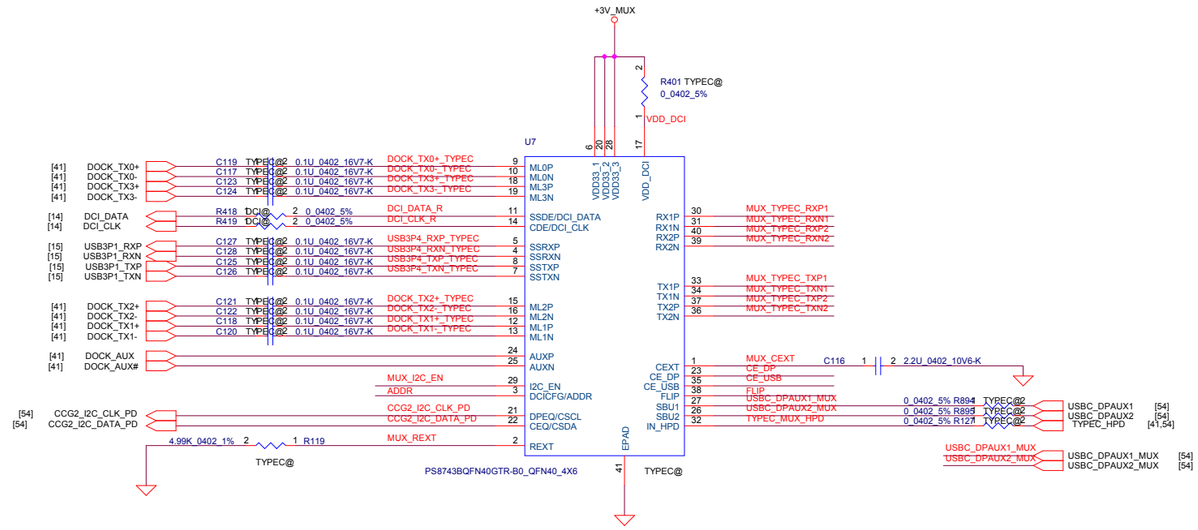
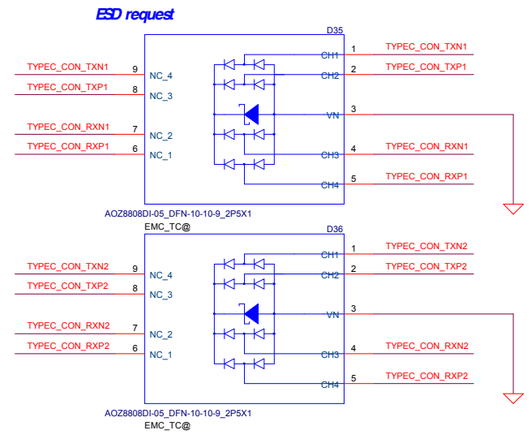
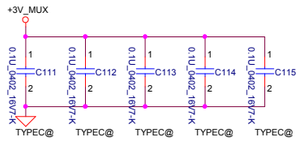
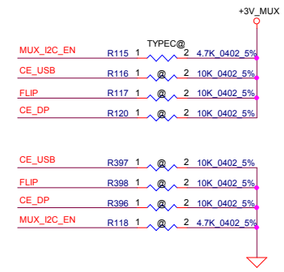
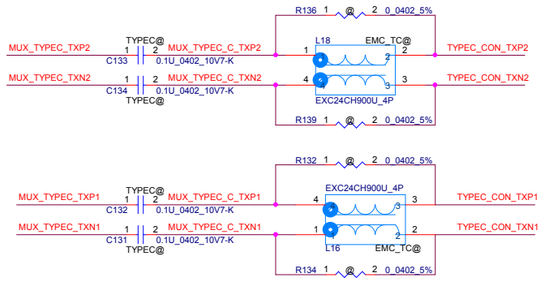
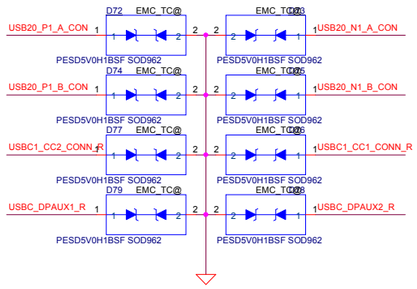


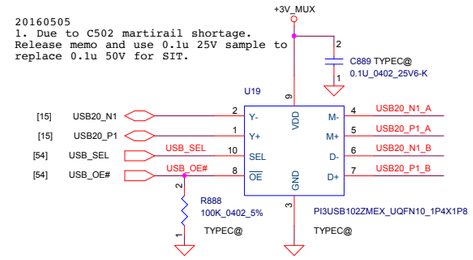


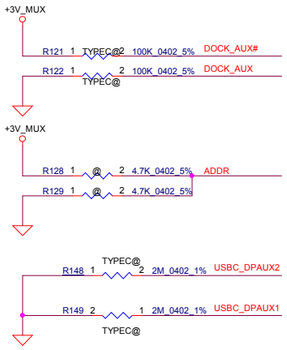


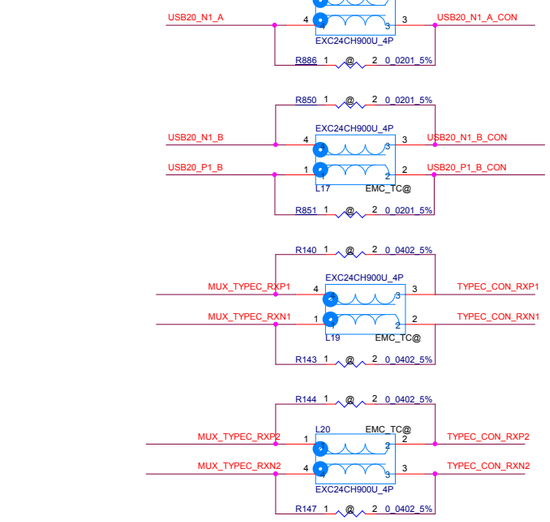










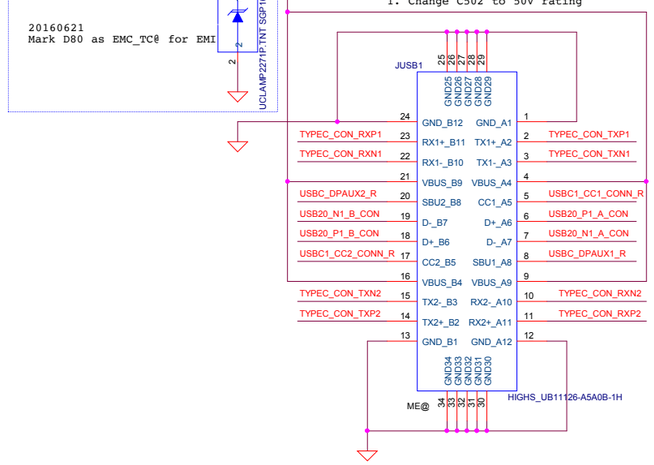


20160414
1. Delete D30,D37 and add D72~D80 for layout placement
2. Add U20 (OVP protection circuit)

20160419
1. Co-lay F11

20160421
1. Change C502 to 50V rating

20160621
Mark D80 as EMC_TC@ for EMI



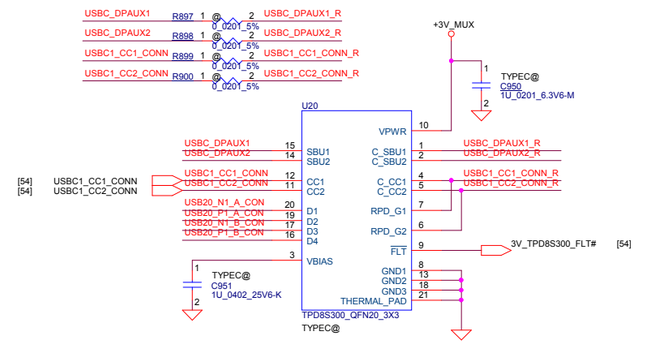
20160330
1.Add CC/SBU protection solution

20160505
1. Unstaff U20 and staff R897,R898,R899,R900 due to U20 martirail shortage.

201616
FLT pin into U5 pin30

20160624
1. Change VPER to +3V_MUX

20160719
1. U20 martirail prepare ready.



Security Classification	LC Future Center Secret Data		
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Title: TYPE-C_MUX

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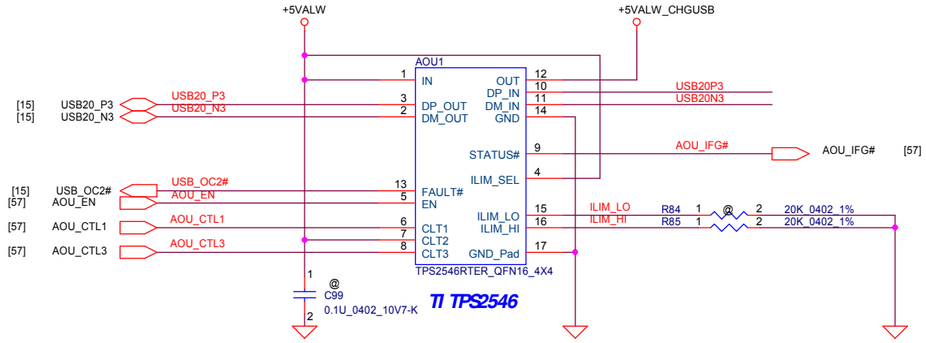
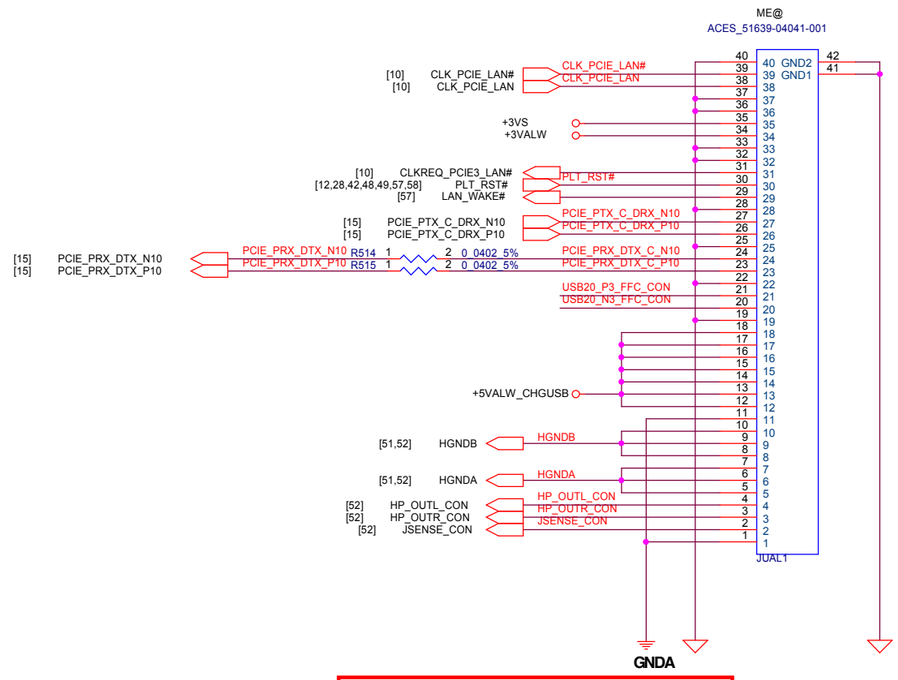


	CLT1	CLT2	CLT3	ILIM_SEL	MOD	
	0	0	0	X	**DCH**	OUT held low
*	1	1	1	1	**CDP**	Data Connected and Port Power Mgt. Function Active
*	1	1	1	0	**SDP2**	Data Connected
*	1	1	0	X	**SDP1**	Data Connected
*	0	1	0	X	**SDP1**	Data Connected
	1	0	0	X	**DCP_Short**	Device Forced to stay in DCP BC 1.2 charging mode
	1	0	1	X	**DCP_Divider**	Device Forced to stay in DCP Divider 1 Charging Mode
*	0	1	1	X	**DCP_Auto**	Data Disconnected and Port Power Mgt. Function Active
	0	0	1	X	**DCP_Auto**	Data Disconnected and Power Wake Function Active



1. AC Capacitor place on Sub/B

Title: **DOCKING/ DCIN CONN**

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20160127
Add TEMBER_DETECT# circuit

20160419
Change RE2 to 18K
for SIT board ID

Vcc	3.3V +/- 5%				
RE1	100K +/- 1%				
Board ID	RE2	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SVT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

All capacitors close to EC

Close to EC

minimum trace width 12 mil

20160307
Stuff CE11 for WRST singal

Un-stuff if not necessary.

1. Version CX : Don't Support Mirror Code
   Version DX/EX/FX : Support Mirror Code
2. For Mirror Code
"H" --> Enable
"L" --> Disable (Default)
*

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Title: EC

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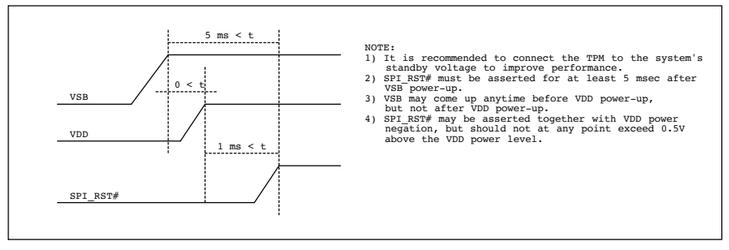
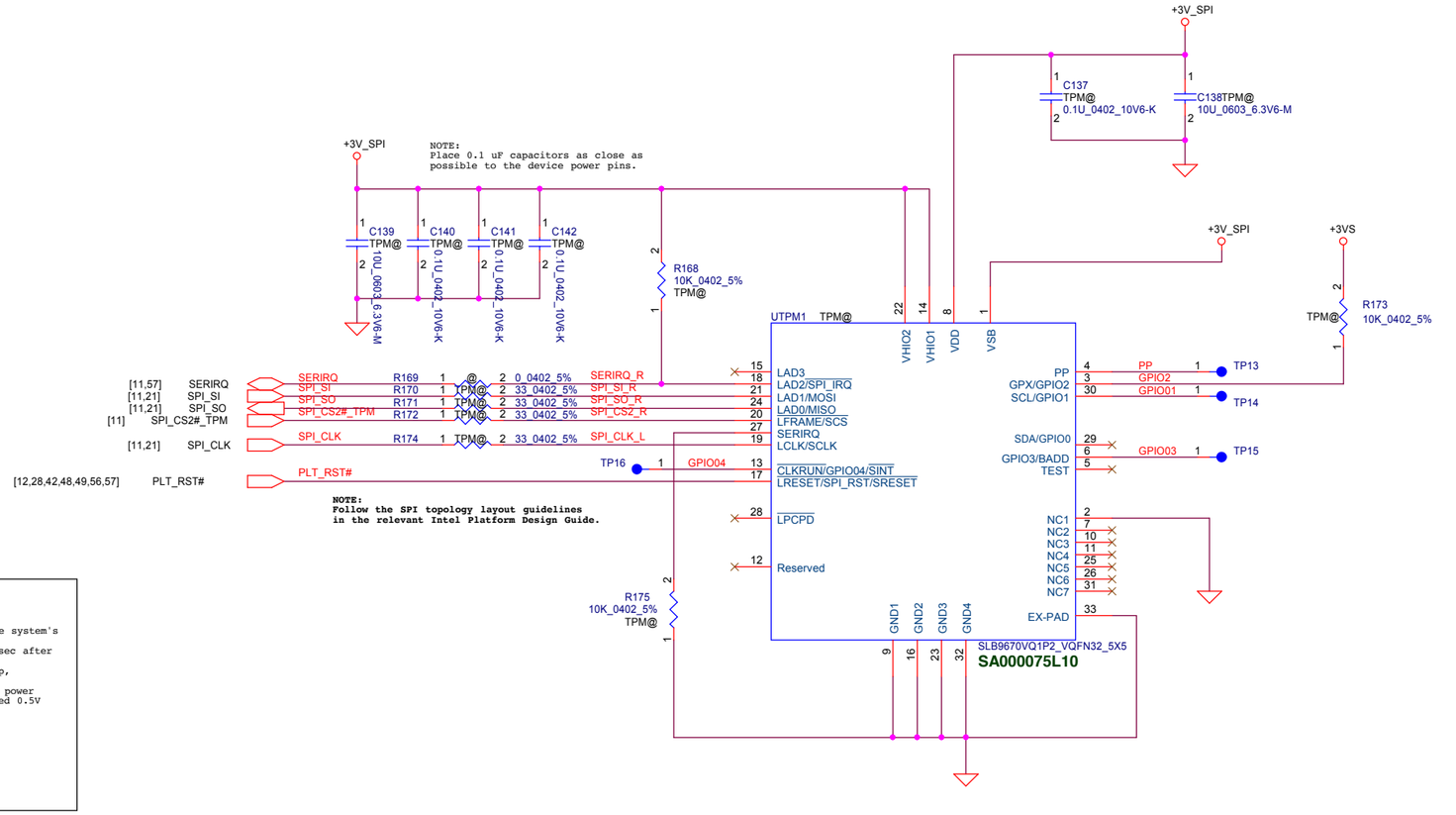
TPM IC

Pin No	TCG PTP Spec (x38)	Infineon SLB9670VQ1.2 FW 6.10	ST Micro ST33HTPM2E32AAB9	Nuvoton NPCT650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	NC	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

Follow THP1_SWG_SIT_EC005, update TPM table

NOTE:
Check timing sequence in SDV phase.





Title		
TPM		
Size: Custom	Document Number: SKYWALKER	Rev: 2.0
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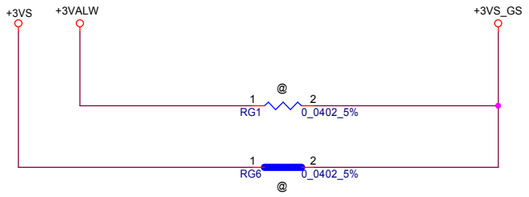


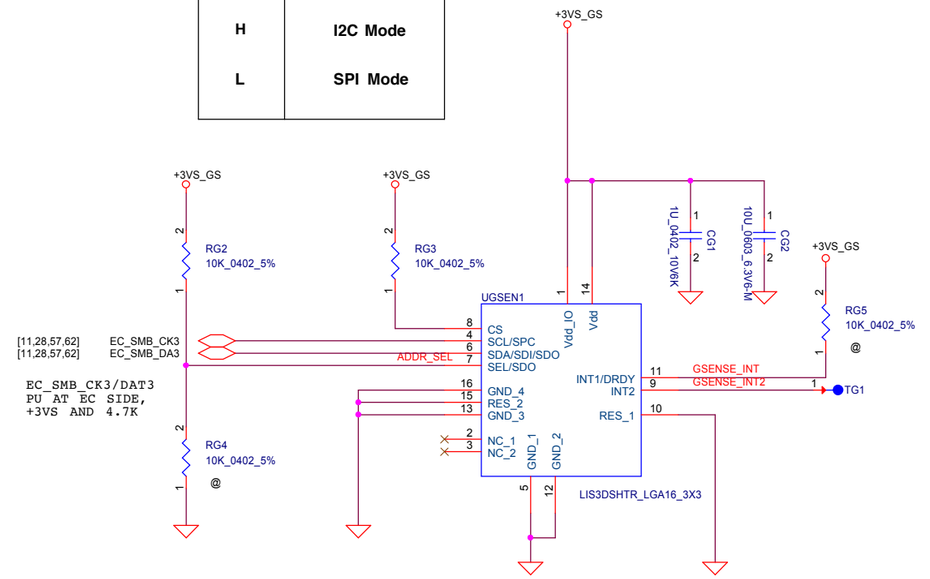
APS G-Sensor

TABLE

P/N	ADDR_SEL	Address
LIS3DSHTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: G SENSOR

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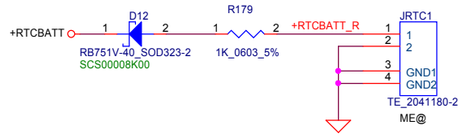
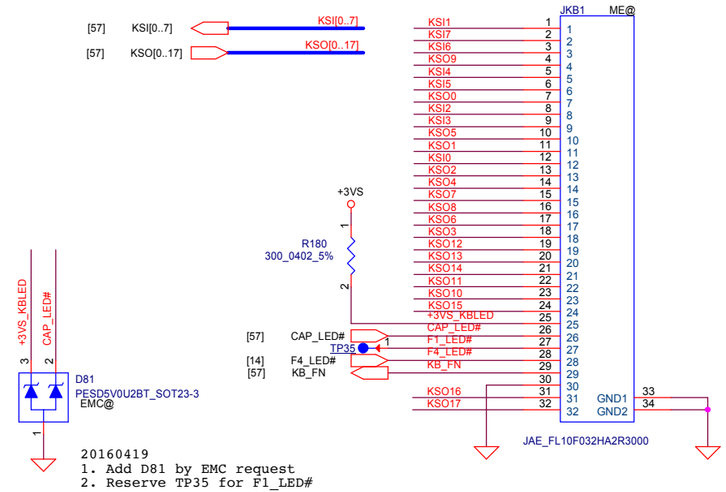
RTC CONN.



KB CONN



20160419
1. Add D81 by EMC request
2. Reserve TP35 for F1_LED#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KB/RTC/TOUCH PAN CONN.

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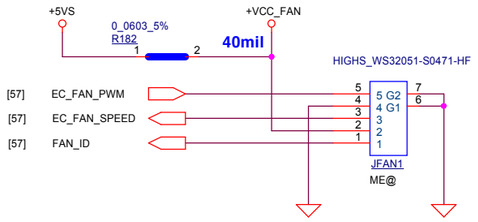
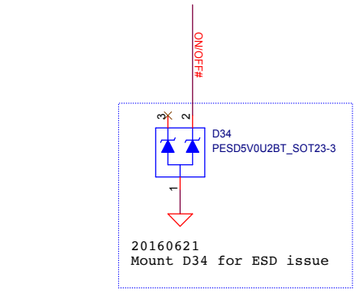
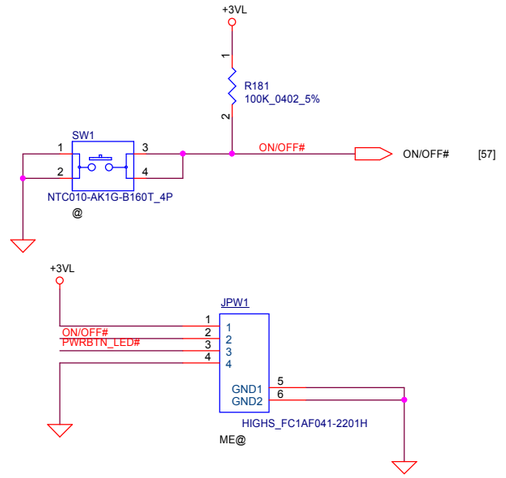
FAN CONN.

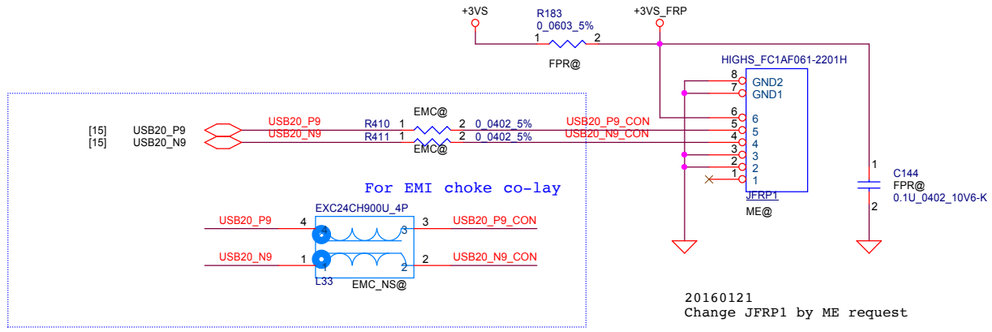


PWR BTN



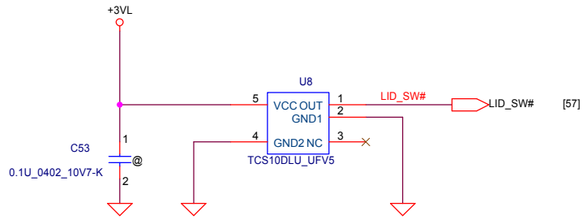


FingerPrint CONN.



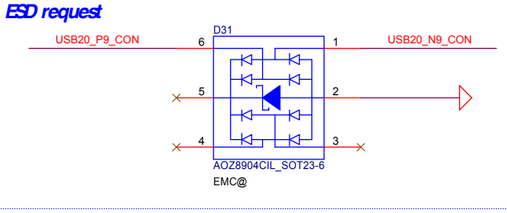
20160121
Change JFRP1 by ME request

Lid Switch



20160420
Delete U17

ESD request



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Title: PBTN/LID/FP/FAN CONN.

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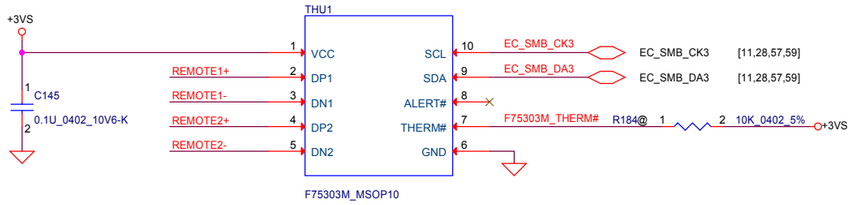
Thermal Sensor placed near by VRAM

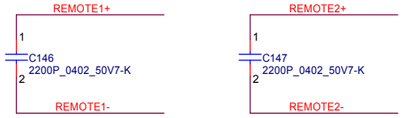


Address 1001_101xb

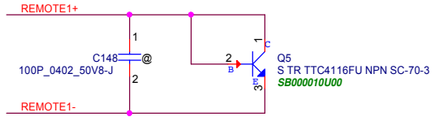
Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

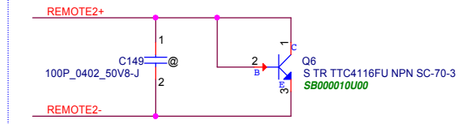
Close to U1

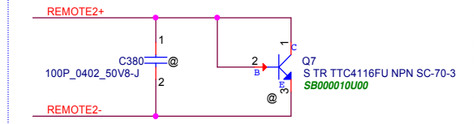


Close to +VCC_CORE



Close to DIMM1&DIMM2





Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: ***Thermal Sensor***

Size	Document Number	Rev
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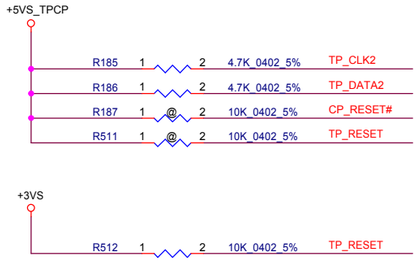
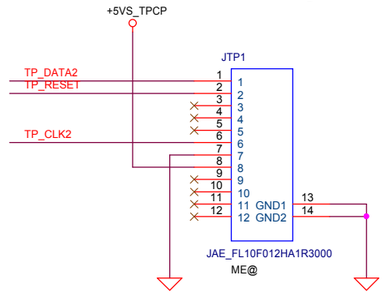
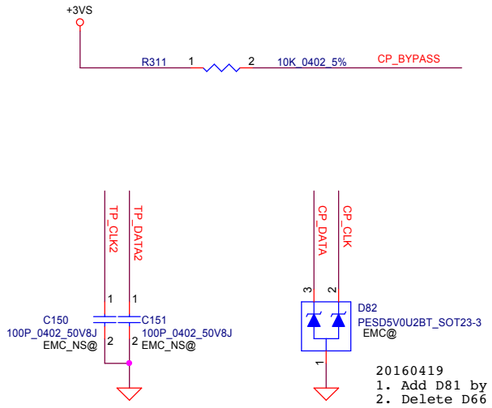


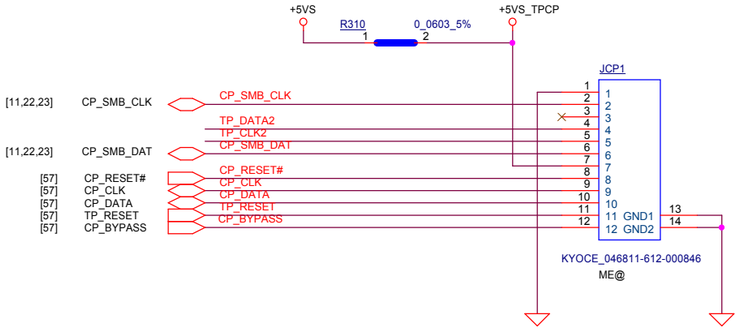
Track point





20160419
1. Add D81 by EMC request
2. Delete D66 and connect to C150/C151

Click Pad



20160417
Change JCP1 to KYOCE_046811-612-000846

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: CP/TPOINTCONN.

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Custom	SKYWALKER	2.0

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Screw Hole

Center Zero

PCB Fedical Mark PAD

Title: P68-PLM/SCREW HOLE

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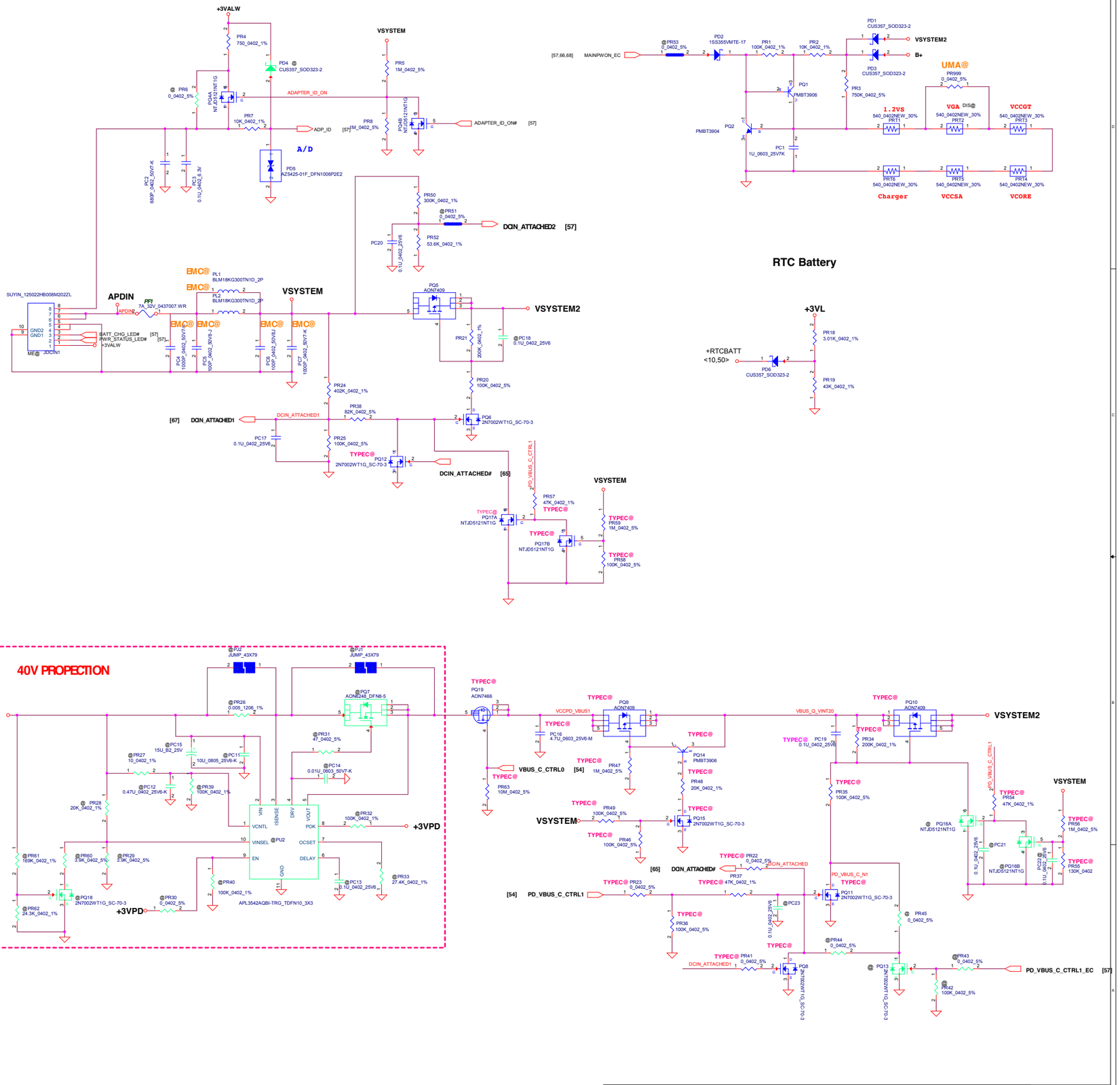

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

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Title: *DCIN / VIN Detector*

LCFC

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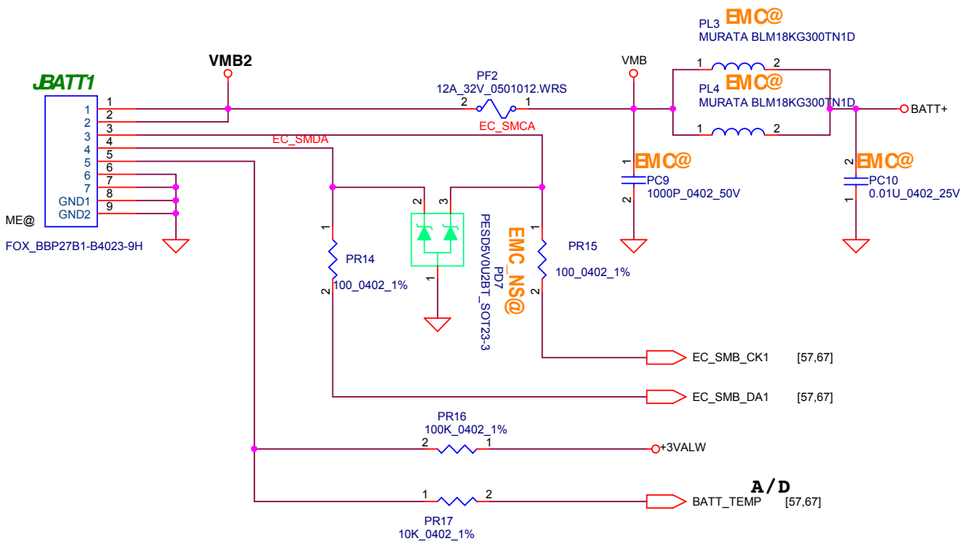
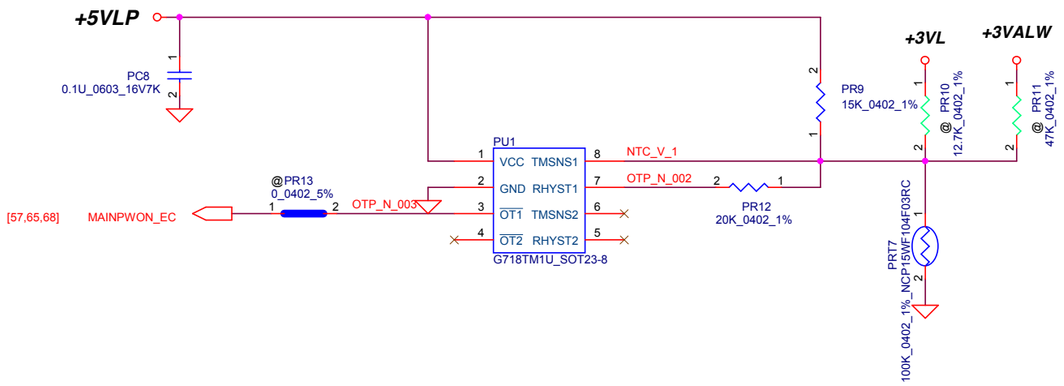


PRT7 under CPU bottom side for CPU thermal protection
This is fot thermal team request



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: ***BATTERY CONN/OTP***

Size: Custom	Document Number: ***Skywalker***	Rev: 2.0
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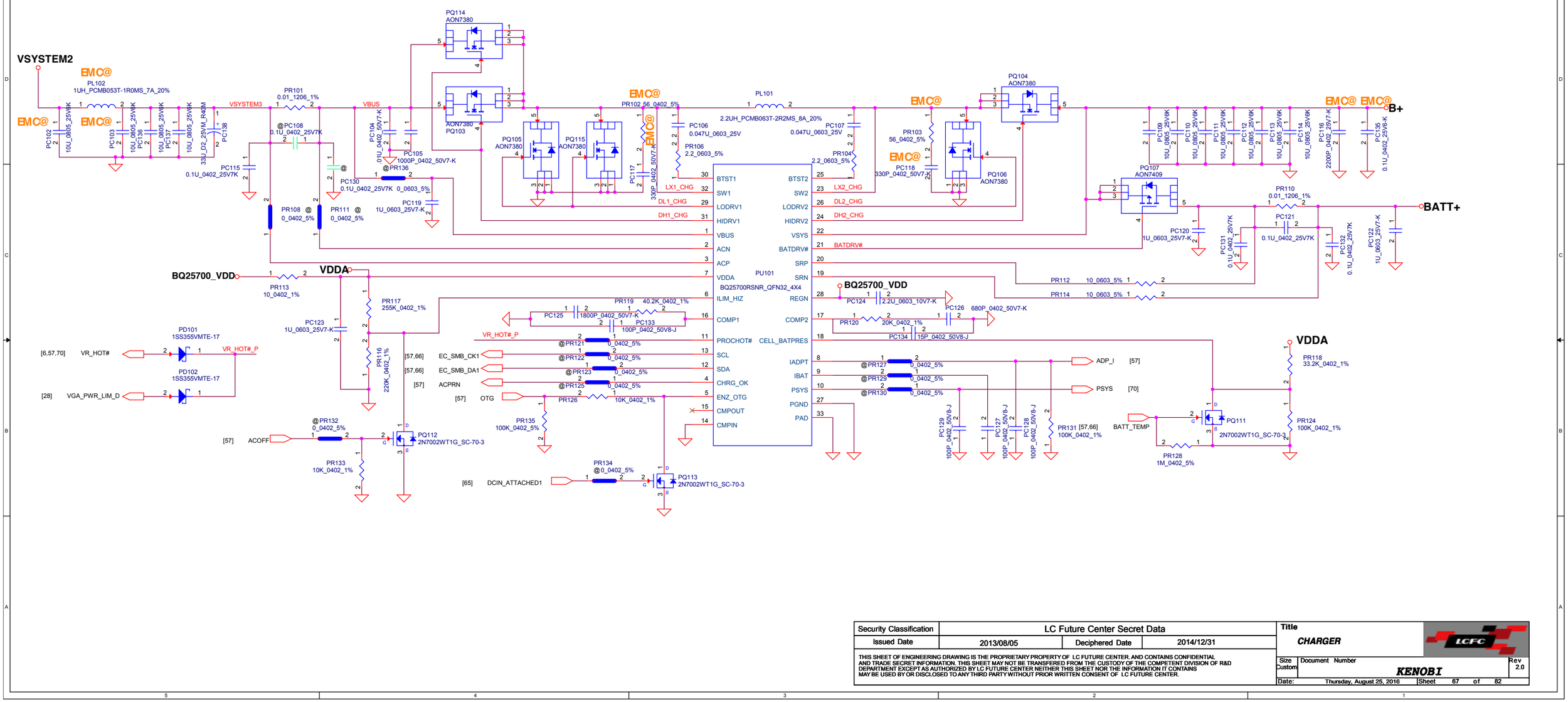

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: CHARGER

Size	Document Number	Rev
Custom	KENOBI	2.0

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+3VALW
FSW=750 KHz
TDC:8A
OCP:11A

+5VALW
FSW=750 KHz
TDC:8A
OCP:11A

6800pf soft start 2ms
47nf soft start 7ms

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: +3VALW/+5VALW

Size: Custom | Document Number: Skywalker | Rev: 2.0

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1.2V
TDC: 12A
OCP: 15A
Fsw: 300KHz

+0.6VS
TDC: 1.5A

B+
PJ304 @JUMP_43X79
B+_1.2V
EMC@ EMC@ RF_NS@ RF_NS@
PC302 10U_0805_25V6-K
PC303 10U_0805_25V6-K
PC304 0.1U_0402_25V6
PC307 2200P_0402_25V
PC305 47P_0402_50V8-J
PC306 68P_0402_50V8J

+1.2VP
EMC@ EMC@
PC312 2200P_0402_25V7-K
PC313 0.1U_0402_25V6
PC311 330U_D2_2V_R9M
PC314 @ 470P_0402_50V7K
PR305 6.04K_0402_1%
PR307 10K_0402_1%
PL301 1UH_PCMC063T-1R0MN_11A_20%
EMC_NS@ PR304 4.7_0603_5%
EMC_NS@ PC317 680P_0402_50V7K
PQ301 AON7408L_DFN8-5
PQ302 AON7380
PR303 2.2_0603_5%
PC310 0.22U_0603_25V7K
DH_1.2V
LX_1.2V
DL_1.2V
FB_1.2V

PU301 RT8231AGQW_WQFN20_3X3
PGND VID CS VLDOIN VTT PAD
BOOT VTTGND
UGATE VTTSNS
PHASE GND
LGATE VTTREF
VDDQ VDD PGOOD
FB TON S5 S3

PR301 100K_0402_1%
PR302 255K_0402_1%
PC301 10U_0603_6.3V6M
+1.2VP
+0.6VSP
PC308 10U_0603_6.3V6M
PC309 0.1U_0402_6.3V7-K
VTTREF_0.6V
PR306 5.1_0603_5%
+5VALW
PC315 0.033U_0402_16V7K
PC316 1U_0402_10VA-K
@PR308 100K_0402_1%
+3VS
PR310 @0_0402_5%
SM_PG_CTRL [7]
@PR311 0_0402_5%
SUSP# [50,57]
PR309 887K_0402_1%
TON_1.2V
S5_1.2V
S3_1.2V
B+_1.2V
PR312 @0_0402_5%
[50,57,78] SYSON
@PR313 47K_0402_5%
@PC318 0.1U_0402_6.3V7-K
@PC319 0.1U_0402_16V

@PJ301 JUMP_43X118
@PJ302 JUMP_43X118
+1.2VP → +1.2V
@PJ303 JUMP_43X39
+0.6VSP → +0.6VS

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +1.2V/+0.6VS
Size: Custom
Document Number: Skywalker
Rev: 2.0
Date: Thursday, August 25, 2016
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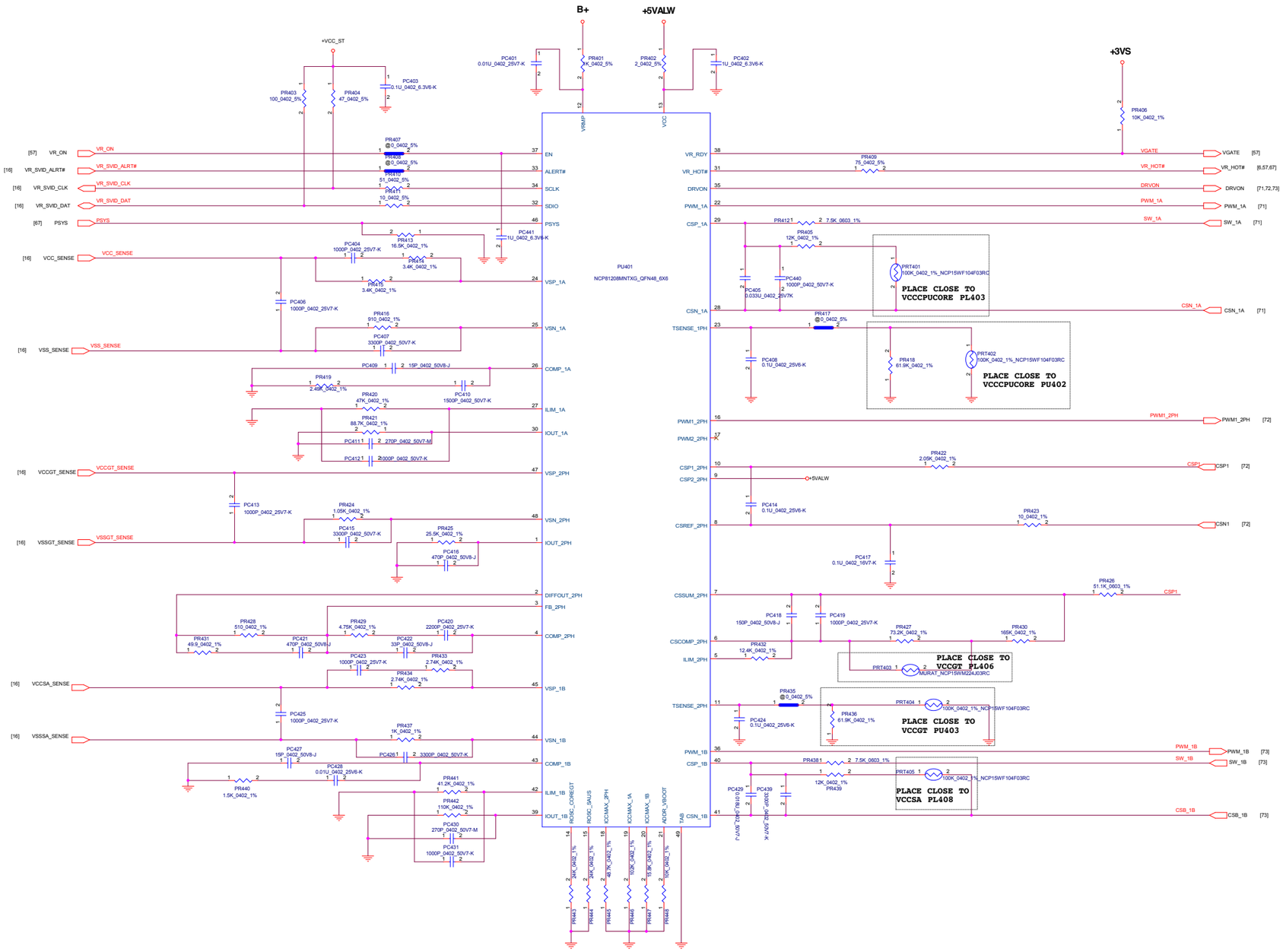

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Issued Date	2013/08/05	Deciphered Date	2014/12/31

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Title	IMVP8		
Size	Document Number		Rev
D	Skywalker		2.0
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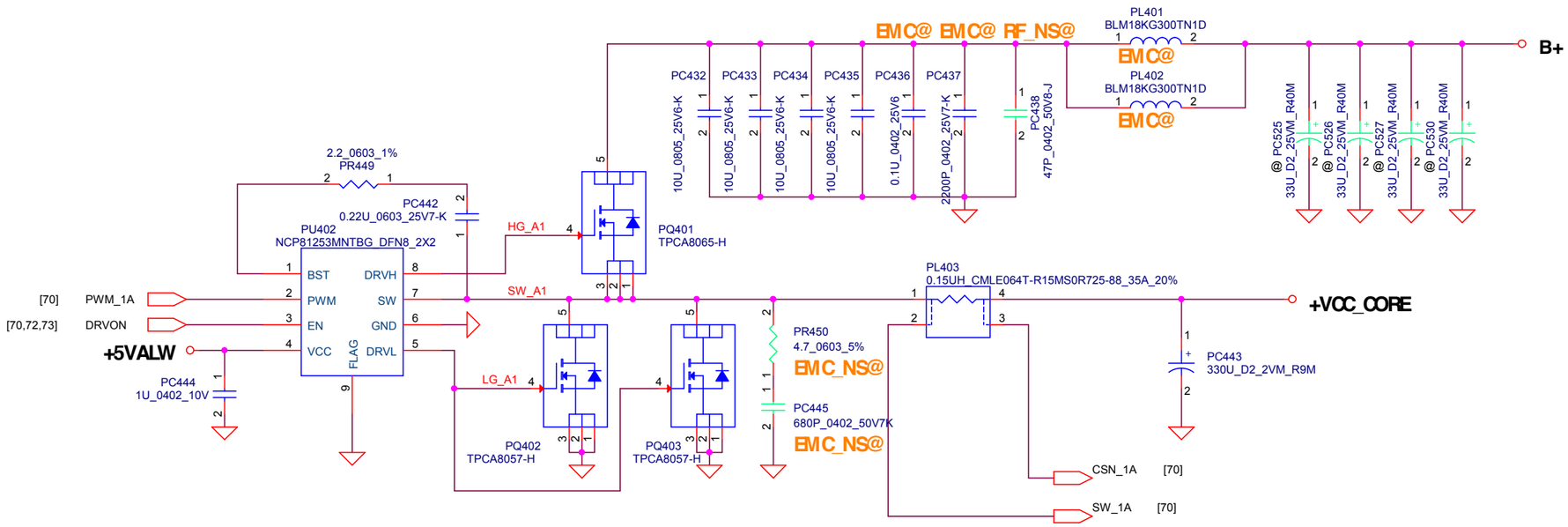

+VCC_CORE
TDC= 21A
IccMAX=31A
OCP = 36A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *+VCC_CORE*

Size	Document Number	Rev
Custom	*Skywalker*	2.0

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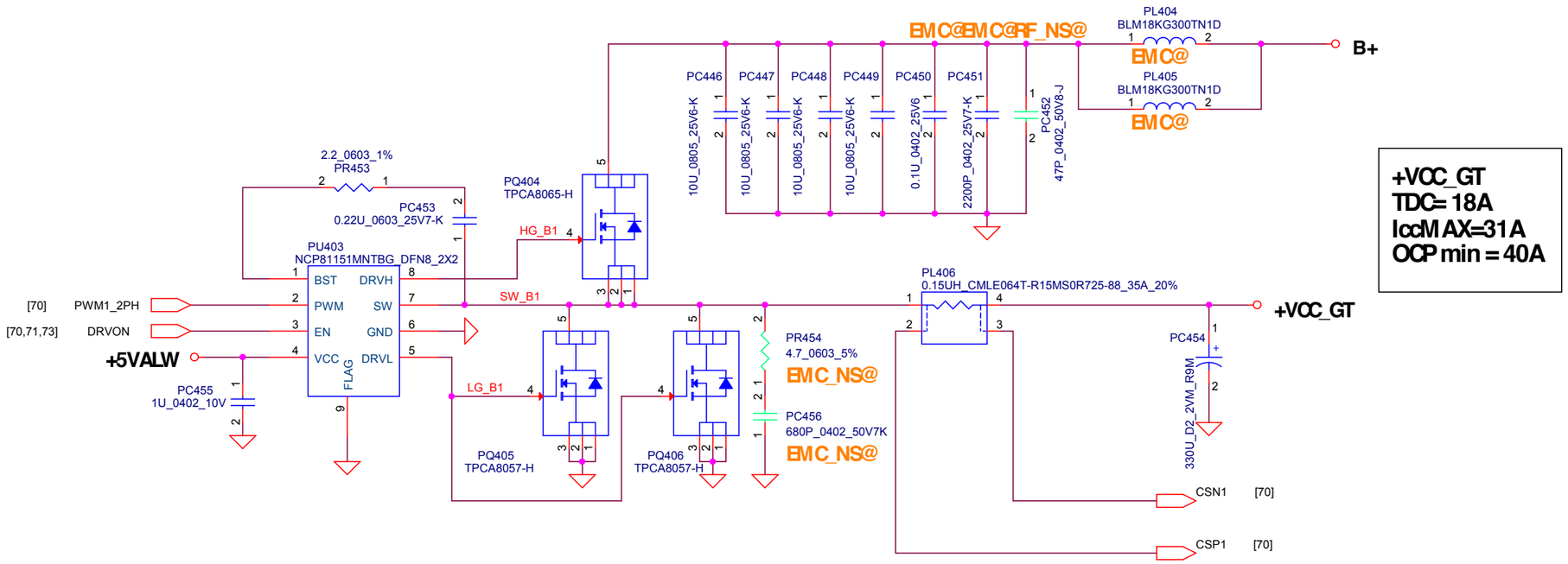

+VCC_GT
TDC= 18A
IccMAX=31A
OCP min = 40A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *+VCC_GT*

Size	Document Number	Rev
Custom	***Skywalker***	2.0

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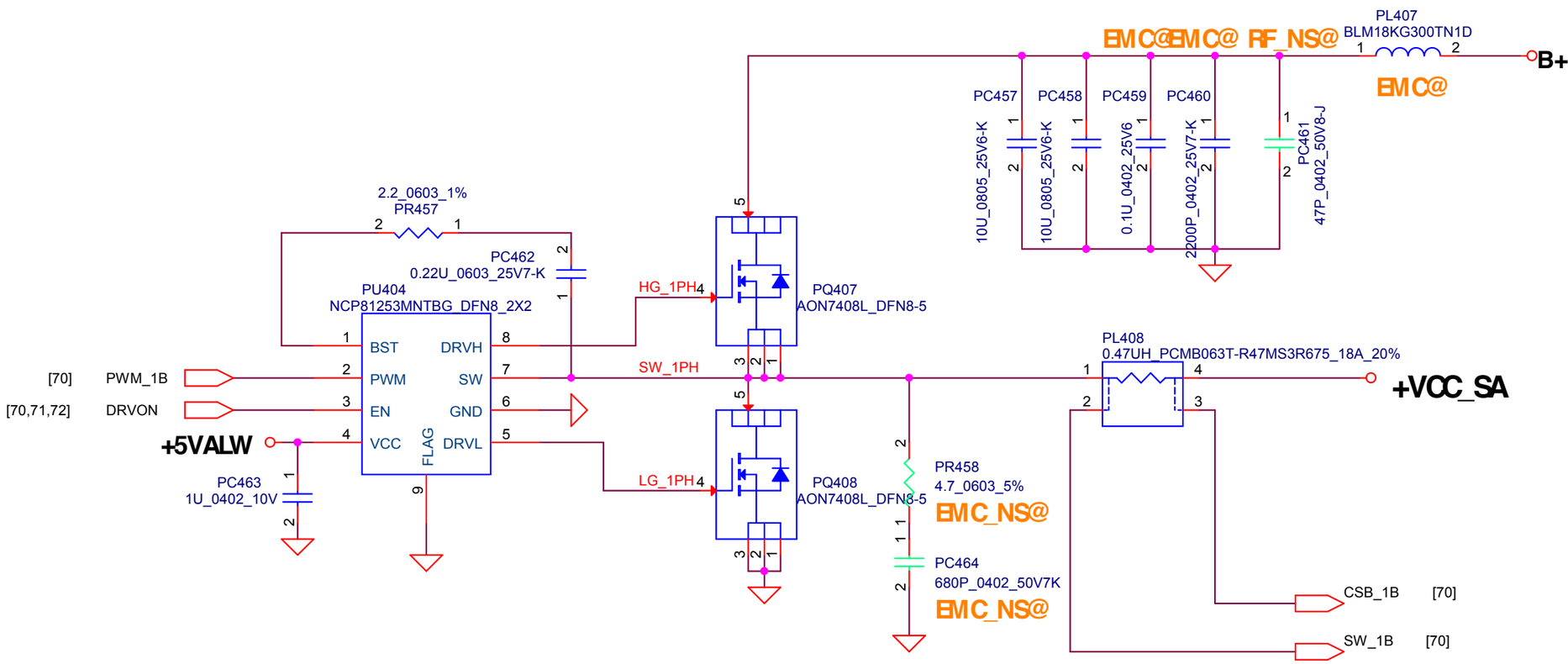

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *+VCC_SA*

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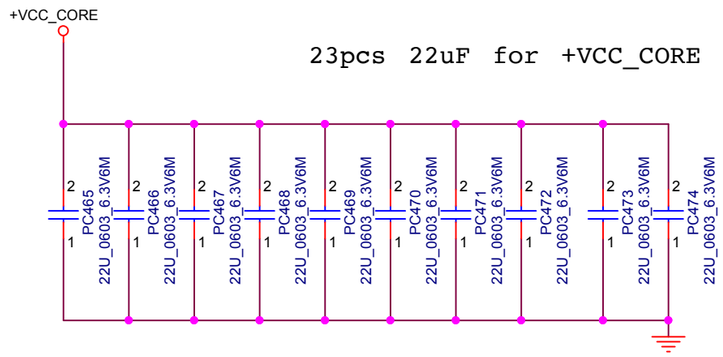
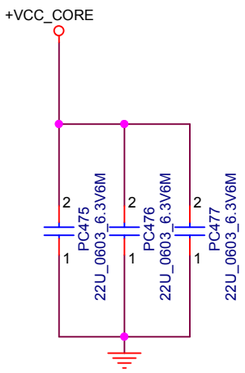
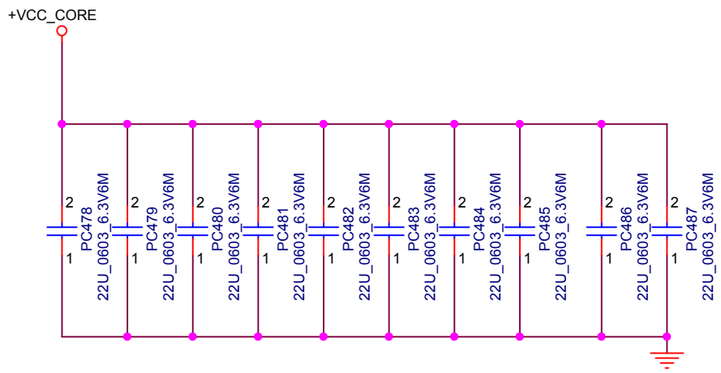
Based on PDDG rev 0.7 Table 5-1.

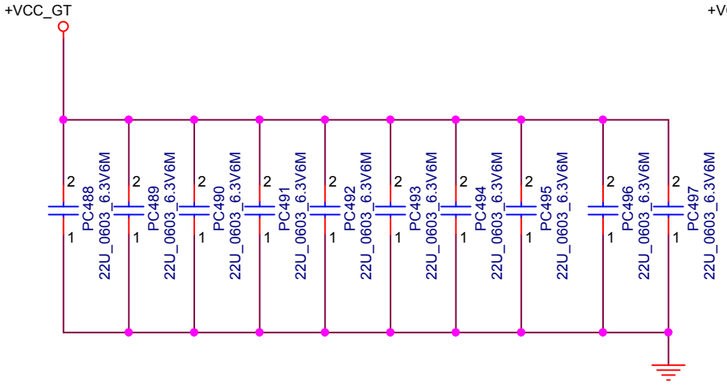
23pcs 22uF for +VCC_CORE

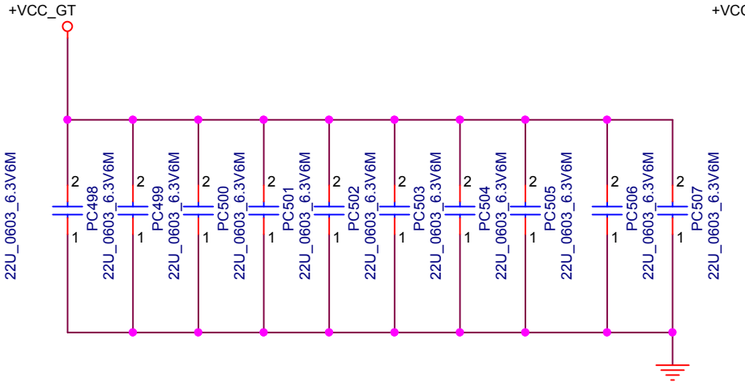


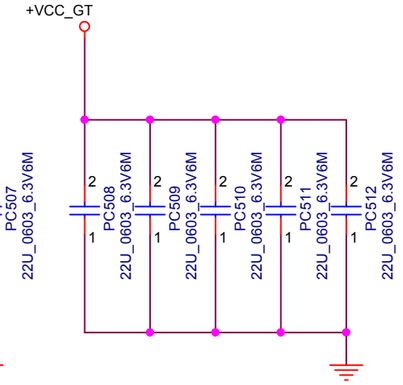




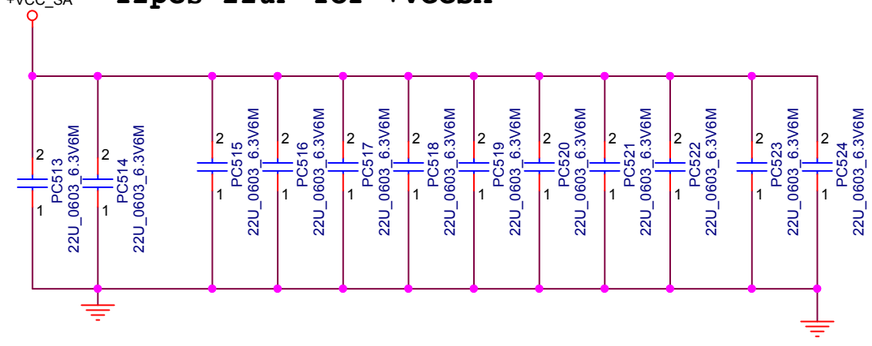
25pcs 22uF for +VCC_GT







12pcs 22uF for +VCCSA



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **PROCESSOR DECOUPLING**

Size	Document Number	Rev
B	Skywalker	2.0

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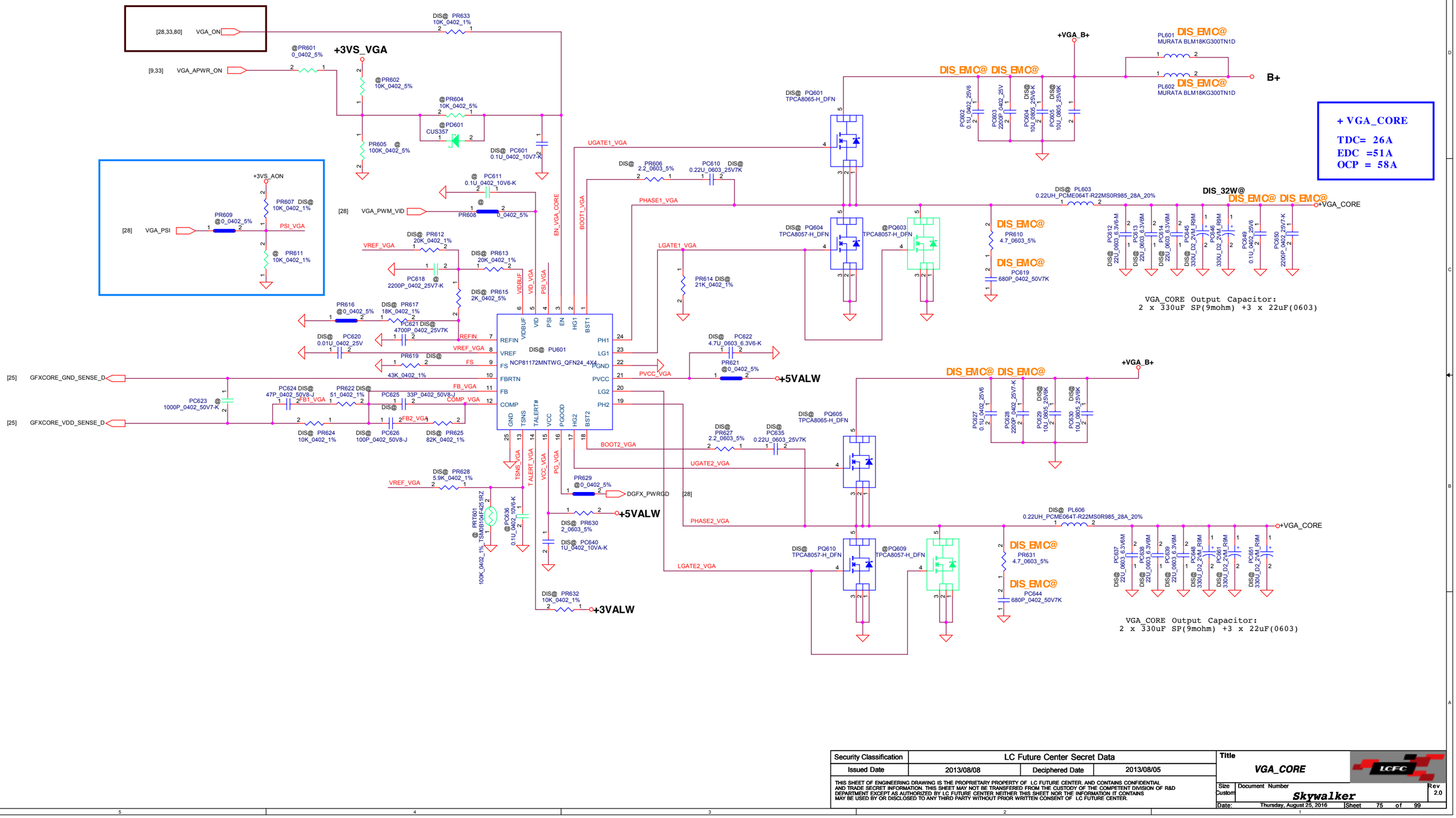

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: VGA_CORE

Size	Document Number	Rev
Custom	Skywalker	2.0

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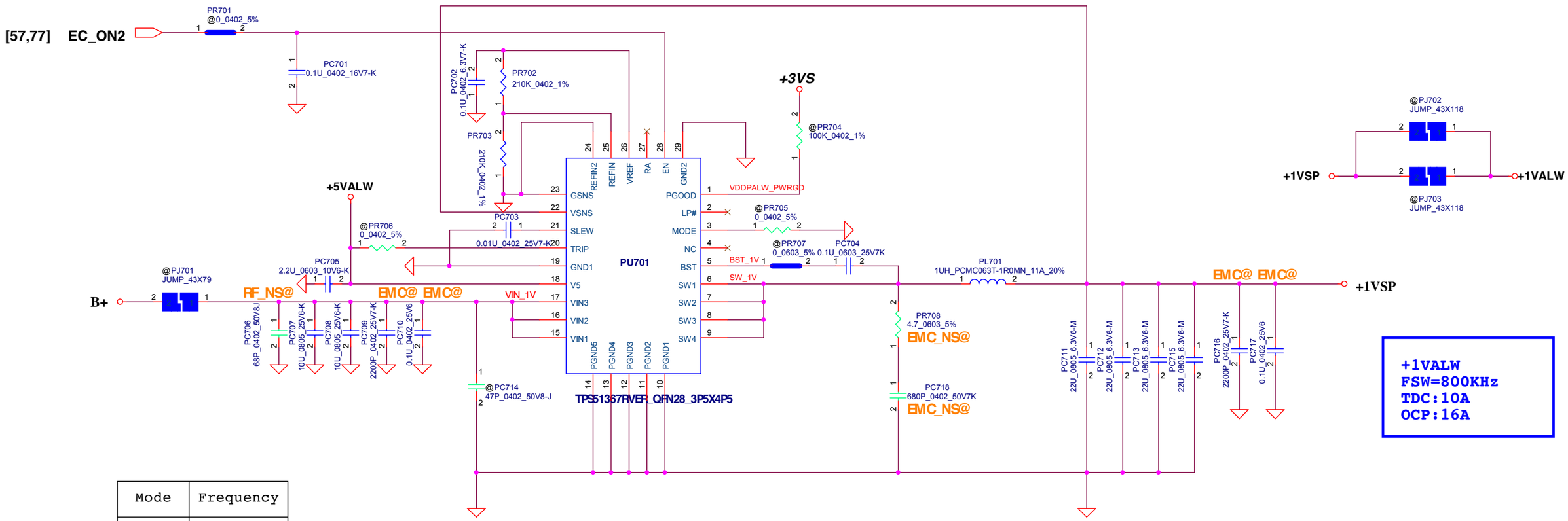

Mode	Frequency
GND	400KHz
Float	800KHz

Title: +1VALW

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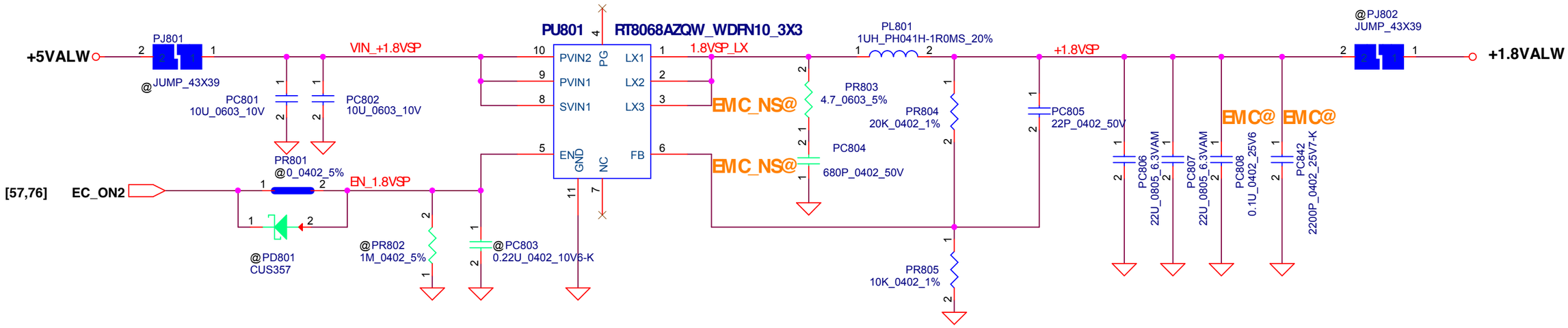
+1.8VALW
TDC: 1A
Fsw: 1MHz



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	*+1.8VALW*		
Size: Custom	Document Number: ***Skywalker***		Rev: 2.0
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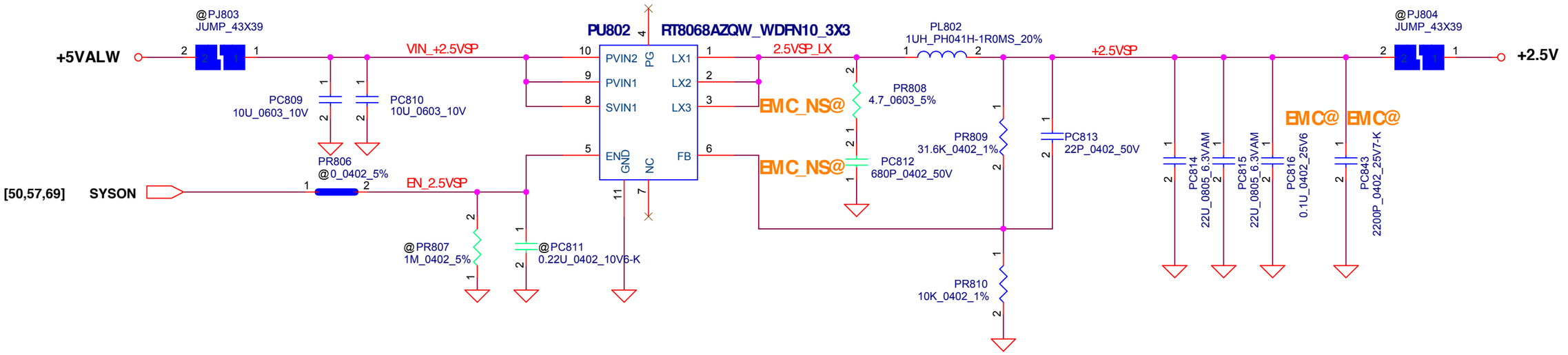
+2.5V
TDC: 2A
Fsw: 1MHz



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	*+2.5V*		
Size: Custom	Document Number: ***Skywalker***		Rev: 2.0
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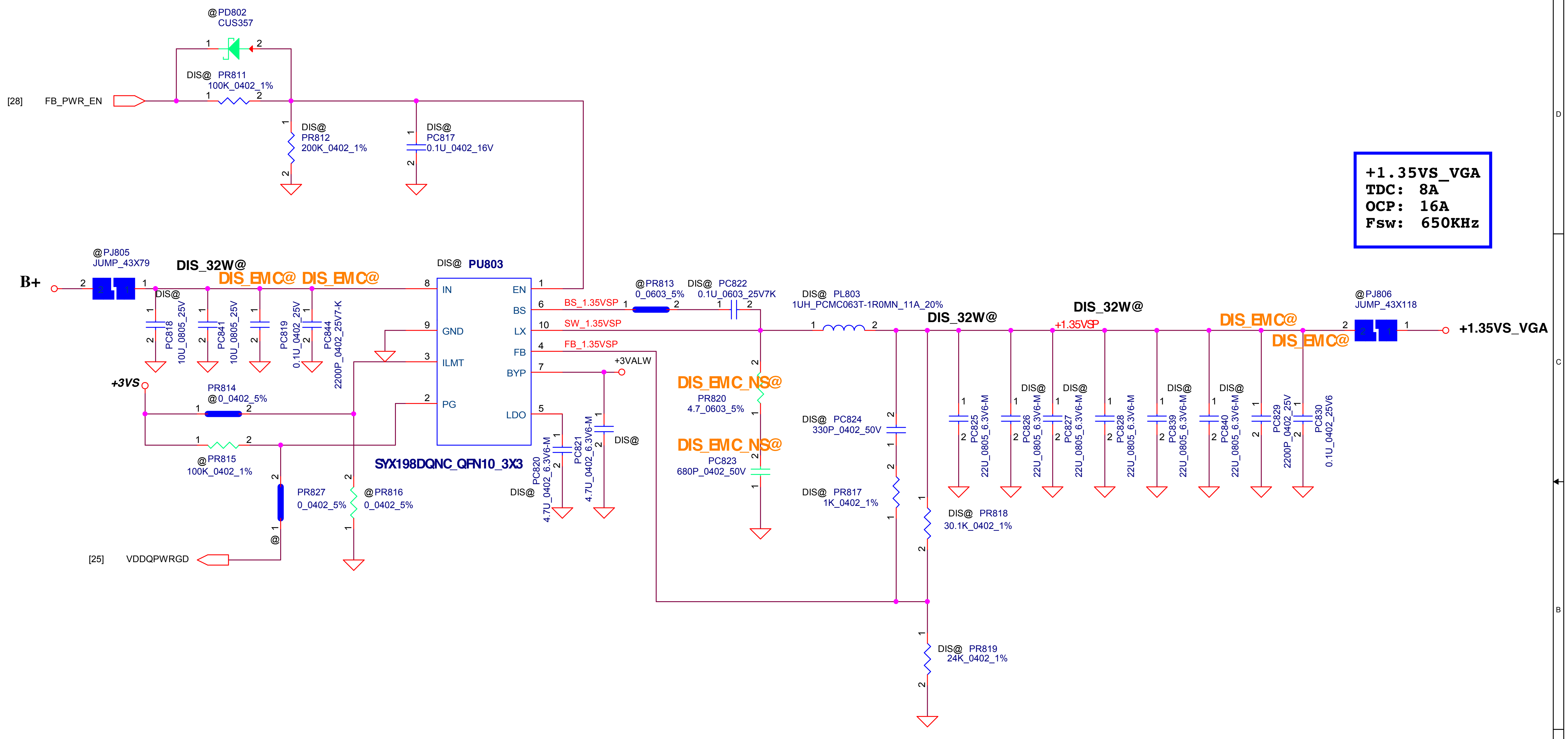


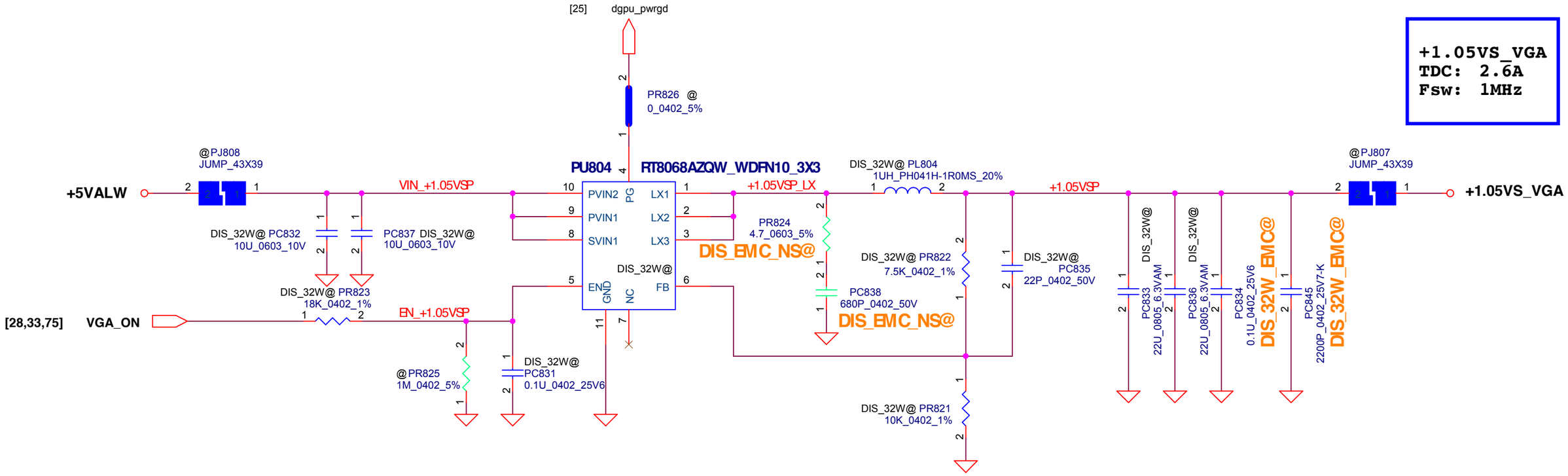
+1.35VS_VGA
TDC: 8A
OCP: 16A
Fsw: 650KHz

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +1.35VS_VGA

Size: Custom | Document Number: Skywalker | Rev: 2.0

Date: Thursday, August 25, 2016 |



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+1.05VS_VGA		
Size	Document Number		Rev
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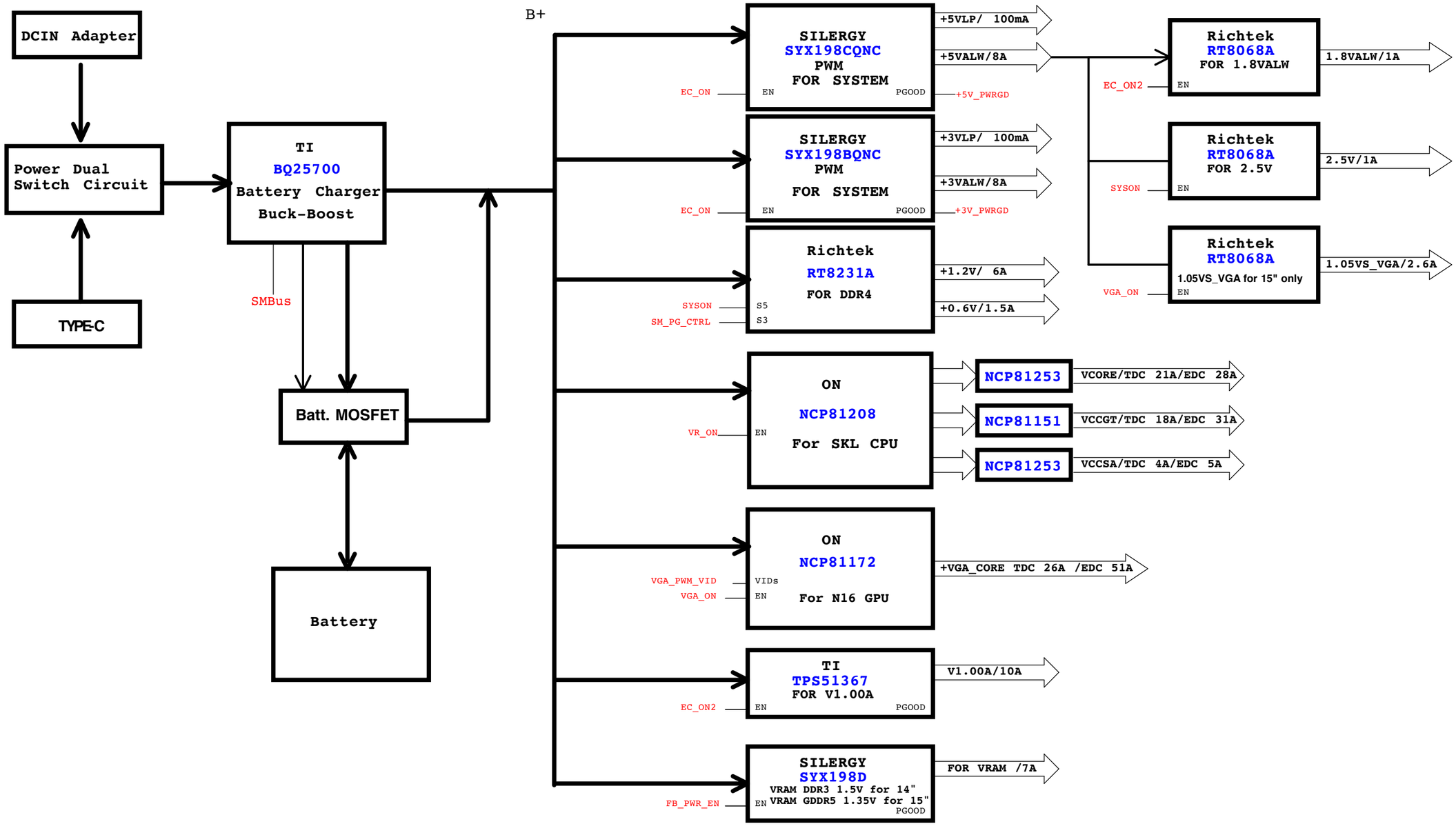

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Issued Date		Deciphered Date	

Title: *Power Block Diagram*

Size	Document Number	Rev
Custom	*Skywalker*	2.0

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Title

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Size	Document Number	Rev
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